AM8EB057A Data Sheet

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1. General Description

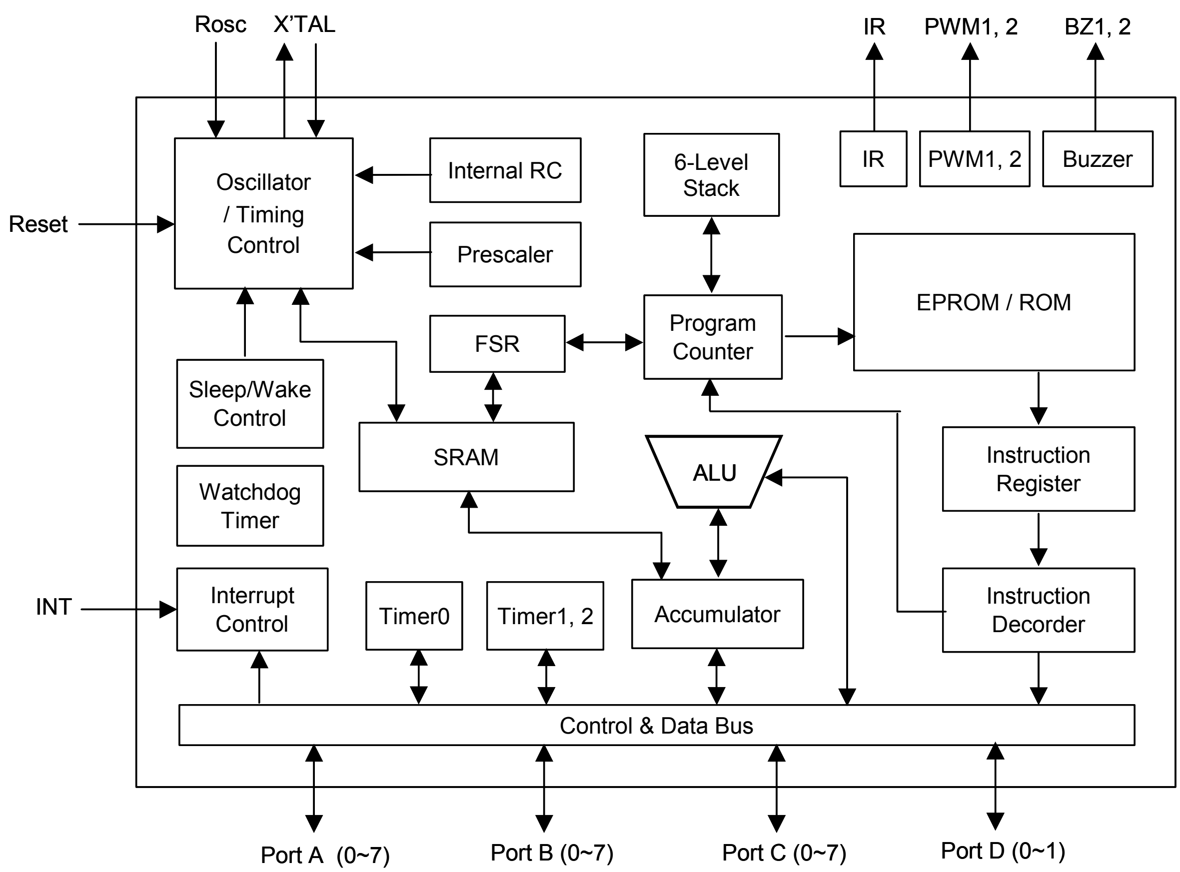
The AM8EB057A is a family of low-cost, high speed, high noise immunity and EPROM-embedded 8-bit CMOS micro-controllers. It employs a RISC architecture with only 55 instructions. All instructions are single cycle except for program branches that take two cycles. The AM8EB057A provide powerful and easy useful instruction set that can directly or indirectly address its register files and data memory.

1.1 Features

- Wide operating voltage range: 2.0 ~ 5.5V at 32kHz, 2.2 ~ 5.5V at DC-4MHz, 2.6 ~ 5.5V at DC-20MHz.
- Wide operating frequency range: 32kHz ~ 20MHz.
- Wide operating temperature range: -40ºC ~ 85ºC.
- ROM: 2K x 14 bits.
- RAM: 144 x 8 bits.
- Selectable oscillator options:
  - IRC: Internal Resistor and Capacitor Oscillator
  - EXT-R: External Resistor and internal Capacitor Oscillator
  - ERC: External Resistor and Capacitor Oscillator
  - LF-XTAL: Low Frequency Crystal Oscillator
  - XTAL: Crystal/Resonator Oscillator
  - HF-XTAL: High Frequency Crystal/Resonator Oscillator
- 6-level deep hardware stack.
- Total 55 single word instructions.
- All instructions are single cycle except for program branches which are two-cycle.
- Direct, indirect addressing modes for data accessing.
- All ROM area LGOTO instruction, all ROM area subroutine LCALL instruction.
- 8-bit real time clock/counter (Timer0) with 8-bit programmable prescaler.
- Two 8-bit re-load or non-stop down-count counter/timer Timer1, Timer2.
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and software Watchdog enable/disable control.
- Internal Power-on Reset (POR).
- Built-in Low Voltage Reset (LVR).
- Power-up Reset Timer (PWRT) and Oscillator Start-up Timer (OST).
- SLEEP mode function to reduce power consumption.
- Four I/O ports PA, PB , PC and PD with independent direction control.
- Software I/O pull-high/pull-down or open-drain control.
- Two 8-bit PWM D/A converters.
- Two Buzzer output.
- One IR carrier output (38k / 57k Hz) with selectable constant-current output.

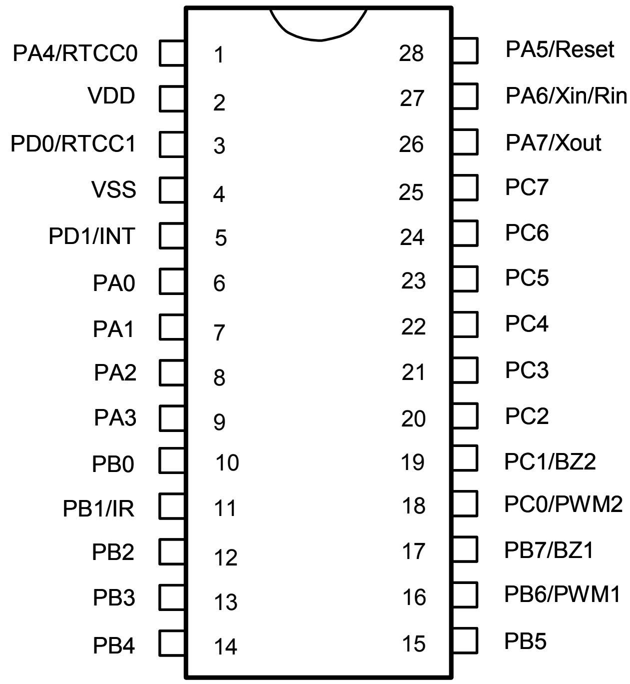
- Six Interrupt source:
  - Timer0 overflow.
  - Timer1 underflow.
  - Timer2 underflow.
  - PB input change.
  - External Interrupt Pin.
  - Watchdog time out Interrupt (If the function is enabled by programming the configuration word.)
- Wake-up from SLEEP by external INT pin or Port B input change.
- Programmable Code Protection.

1.2 Block Diagram



1.3 Pin Assignment

28-pin PDIP, SOP, SSOP



1.4 Pin Description

Name	ATTR.	Function
PA0~PA3	I/O	PA0~PA3 are bi-directional I/O port.
PA4/RTCC0	I/O	Bi-directional PA4. Input pin of real time counter Timer0, Timer1/clock.
PA5/Reset	I/O	Bi-directional PA5. Input pin for device reset. If this pin is low, the device is reset
PA6/Xin/Rin	I/O	X'TAL type: Input terminal of crystal oscillator. EXT-R type: External resistor for EXT-R oscillator; ERC type: Input pin of external RC oscillator. IRC type: Bi-directional PA6.
PA7/Xout	I/O	X'TAL type: Output terminal of crystal oscillator. EXT-R or ERC type: This pin can output instruction clock. IRC type: Bi-directional PA7, or this pin can output instruction clock.
PB0	I/O	Bi-directional PB0.
PB1/IR	I/O	Bi-directional PB1. IR carrier output.
PB2~PB5	I/O	PB2~PB5 are bi-directional I/O port.

Name	ATTR.	Function
PB6/PWM1	I/O	Bi-directional PB6. PWM1 output.
PB7/BZ1	I/O	Bi-directional PB7. Buzzer1 output.
PC0/PWM2	I/O	Bi-directional PC0. PWM2 output.
PC1/BZ2	I/O	Bi-directional PC1. Buzzer2 output.
PC2~PC7	I/O	PC2~PC7 are bi-directional I/O port.
PD0/RTCC1	I/O	Bi-directional PD0. Input pin of real time counter Timer2.
PD1/INT	I/O	Bi-directional PD1. External interrupt input.
VDD	-	Power supply.
VSS	-	Ground.

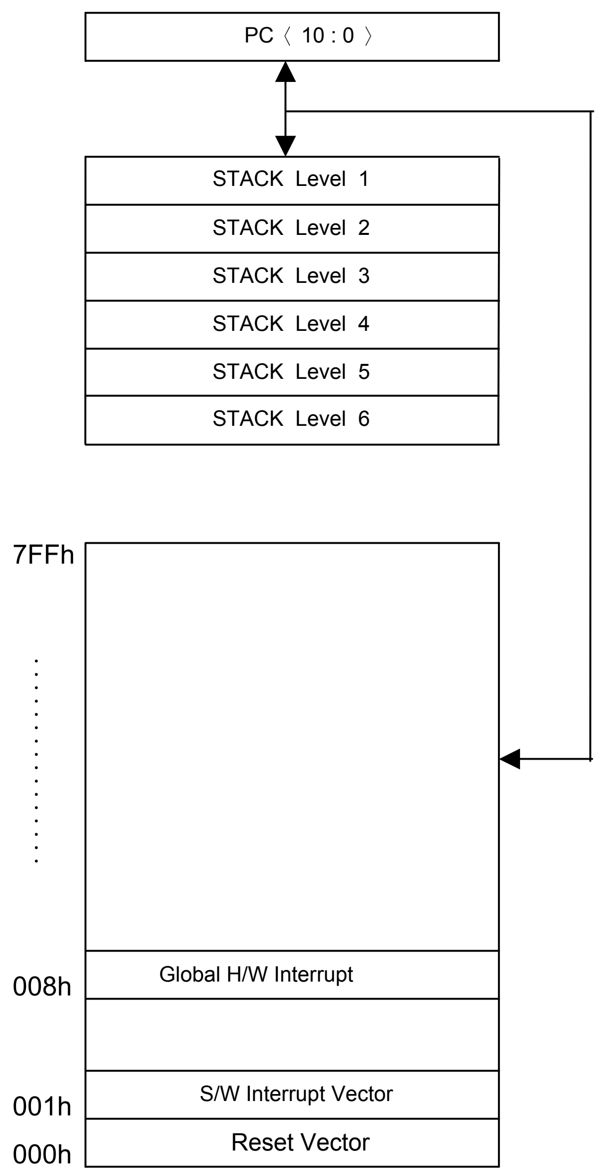
2. Memory Organization

AM8EB057A memory is organized into program memory and data memory.

2.1 Program Memory Organization

The AM8EB057A has a 11-bit Program Counter (PC) capable of addressing a 2K×14 bit program memory space. The RESET vector of the AM8EB057A is at 000h; The INT instruction software interrupt vector is at 001h; The Global hardware interrupt vector is at 008h. AM8EB057A supports all ROM area LCALL/LGOTO instructions without page.

FIGURE 2.1: Program Memory Map and STACK



2.2 Data Memory Map

Data memory includes General Function Registers and General Storage Registers. The Data Memory are accessed either directly or indirectly through the FSR register.

TABLE 2.1: Registers File Map for AM8EB057

<table>
<tr><th>Address</th><th>Description</th><th></th><th></th><th></th></tr>
<tr><td>00h</td><td>Indirect Addressing Register</td><td></td><td></td><td></td></tr>
<tr><td>01h</td><td>Timer0</td><td></td><td></td><td></td></tr>
<tr><td>02h</td><td>PCL</td><td></td><td></td><td></td></tr>
<tr><td>03h</td><td>STATUS</td><td></td><td></td><td></td></tr>
<tr><td>04h</td><td>FSR</td><td></td><td></td><td></td></tr>
<tr><td>05h</td><td>PortA</td><td></td><td></td><td></td></tr>
<tr><td>06h</td><td>PortB</td><td></td><td></td><td></td></tr>
<tr><td>07h</td><td>PortC</td><td></td><td></td><td></td></tr>
<tr><td>08h</td><td>PortD</td><td></td><td></td><td></td></tr>
<tr><td>09h</td><td>PortC PH</td><td></td><td></td><td></td></tr>
<tr><td>0Ah</td><td>PortC PD</td><td></td><td></td><td></td></tr>
<tr><td>0Bh</td><td>PortC OD</td><td></td><td></td><td></td></tr>
<tr><td>0Ch</td><td>PortD Control</td><td></td><td></td><td></td></tr>
<tr><td>0Fh</td><td>Interrupt Status Register</td><td></td><td></td><td></td></tr>
<tr><td>10h ~ 1Fh</td><td>16 Bytes SRAM</td><td></td><td></td><td></td></tr>
<tr><td>20h ~ 3Fh</td><td>32 Bytes SRAM
(Bank 0)</td><td>32 Bytes SRAM
(Bank 1)</td><td>32 Bytes SRAM
(Bank 2)</td><td>32 Bytes SRAM
(Bank 3)</td></tr>
</table>

3. Functional Descriptions

3.1 General Function Registers

- **INAR (Indirect Address Register): R0**

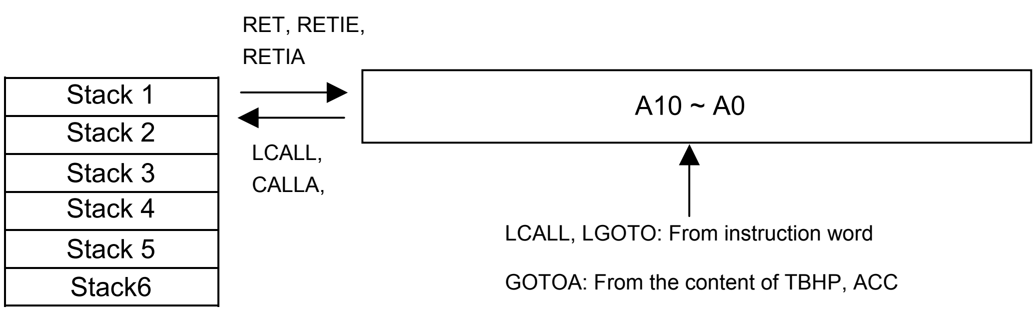
  R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction accessing this register can access data pointed by FSR(R4).

- **Timer0 (8-bit real-time clock/timer): R1**

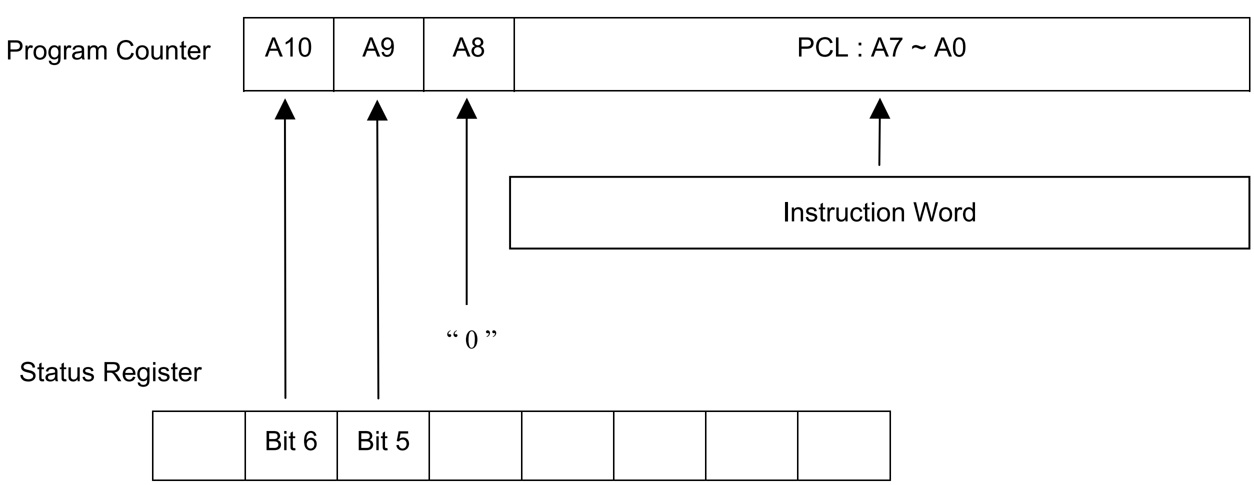
  This register increases by an external signal edge applied to RTCC0 pin, or by internal instruction cycle. It can be read or written as any other register.

- **PCL (Low Byte of Program Counter): R2**

  This register increases itself every instruction cycle, except the following condition shown in Figure below.



For change content of PCL register instruction where the PCL register is the destination, the Bit5 and Bit6 of the Status register will provide data to A9 and A10 of the Program Counter, The A8 of the Program Counter is always cleared. The configuration is shown in following figure .



- **STATUS (Status Register): R3**

The content of R3 is listed in Table below.

TABLE 3.1: STATUS Register

Bit	Symbol	Description
0	C	Carry/borrow bit ADD = 1, A carry occurred = 0, A carry did not occur SUB = 1, A borrow did not occur = 0, A borrow occur
1	DC	Half carry/half borrow bit ADD = 1, A carry from the 4th low order bit of the result occurred = 0, A carry from the 4th low order bit of the result did not occur SUB = 1, A borrow from the 4th low order bit of the result did not occur = 0, A borrow from the 4th low order bit of the result occurred
2	Z	Zero bit = 1, The result of a logic operation is zero = 0, The result of a logic operation is not zero
3	PD	Power down flag bit = 1, After power-up or by the CLRWDT instruction = 0, By the SLEEP instruction
4	TO	Time overflow flag bit = 1, After power-up or by the CLRWDT or SLEEP instruction = 0, A WDT time-overflow occurred
5	PA0	Program Page Pre-select Bit PA1, PA0 = 00, Program Page 0 (000h ~ 1FFh) PA1, PA0 = 01, Program Page 1 (200h ~ 3FFh) PA1, PA0 = 10, Program Page 2 (400h ~ 5FFh) PA1, PA0 = 11, Program Page 3 (600h ~ 7FFh)
6	PA1	
7	-	General purpose R/W bits

- **FSR (File select register pointer): R4**

Bit 0~5 are used to select up to 64 registers (address: 00h~3Fh) in the indirect addressing mode; Bit 6~7 are used to select SRAM bank, shown in following Figure,

B7	B6

SRAM Bank select

B5	B4	B3	B2	B1	B0

Indirect Addressing Mode location select

00h	INAR
01h	Timer0
02h	PCL
03h	STATUS
04h	FSR
05h	PortA
06h	PortB
07h	PortC
08h	PortD

09h	PortC PH			
0Ah	PortC PD			
0Bh	PortC OD			
0Ch	PortD Control			
0Fh	Interrupt Status Register			
10h ~ 1Fh	16 Bytes SRAM			
20h ~ 3Fh	32 Bytes SRAM (Bank 0)	32 Bytes SRAM (Bank 1)	32 Bytes SRAM (Bank 2)	32 Bytes SRAM (Bank 3)

- **PORT A: R5**

  PA7:PA0, bi-directional I/O Register.

- **PORT B: R6**

  PB7:PB0, bi-directional I/O Register.

- **PORT C: R7**

  PC7:PC0, bi-directional I/O Register.

- **PORT D: R8**

  PD1, PD0, bi-directional I/O Register.

- **PortC Pull High Control Register: R9**

  The R9 register is both readable and writable.

  * Bit 0 (/PHC0) : = 0, Enable the internal pull-high of PC0 pin.
  = 1, Disable the internal pull-high of PC0 pin.
  * Bit 1 (/PHC1) : = 0, Enable the internal pull-high of PC1 pin.
  = 1, Disable the internal pull-high of PC1 pin.
  * Bit 2 (/PHC2) : = 0, Enable the internal pull-high of PC2 pin.
  = 1, Disable the internal pull-high of PC2 pin.
  * Bit 3 (/PHC3) : = 0, Enable the internal pull-high of PC3 pin.
  = 1, Disable the internal pull-high of PC3 pin.
  * Bit 4 (/PHC4) : = 0, Enable the internal pull-high of PC4 pin.
  = 1, Disable the internal pull-high of PC4 pin.
  * Bit 5 (/PHC5) : = 0, Enable the internal pull-high of PC5 pin.
  = 1, Disable the internal pull-high of PC5 pin.
  * Bit 6 (/PHC6) : = 0, Enable the internal pull-high of PC6 pin.
  = 1, Disable the internal pull-high of PC6 pin.
  * Bit 7 (/PHC7) : = 0, Enable the internal pull-high of PC7 pin.
  = 1, Disable the internal pull-high of PC7 pin

- **PortC Pull Down Control Register: RA**

  The RA register is both readable and writable.

  * Bit 0 (/PDC0) : = 0, Enable the internal pull-down of PC0 pin.
    = 1, Disable the internal pull-down of PC0 pin.
  * Bit 1 (/PDC1) : = 0, Enable the internal pull-down of PC1 pin.
    = 1, Disable the internal pull-down of PC1 pin.
  * Bit 2 (/PDC2) : = 0, Enable the internal pull-down of PC2 pin.
    = 1, Disable the internal pull-down of PC2 pin.
  * Bit 3 (/PDC3) : = 0, Enable the internal pull-down of PC3 pin.
    = 1, Disable the internal pull-down of PC3 pin.
  * Bit 4 (/PDC4) : = 0, Enable the internal pull-down of PC4 pin.
    = 1, Disable the internal pull-down of PC4 pin.
  * Bit 5 (/PDC5) : = 0, Enable the internal pull-down of PC5 pin.
    = 1, Disable the internal pull-down of PC5 pin.
  * Bit 6 (/PDC6) : = 0, Enable the internal pull-down of PC6 pin.
    = 1, Disable the internal pull-down of PC6 pin.
  * Bit 7 (/PDC7) : = 0, Enable the internal pull-down of PC7 pin.
    = 1, Disable the internal pull-down of PC7 pin

- **PortC Open Drain Control Register: RB**

  The RB register is both readable and writable.

  * Bit 0 (ODC0) : = 0, Disable the internal open-drain of PC0 pin.
    = 1, Enable the internal open-drain of PC0 pin.
  * Bit 1 (ODC1) : = 0, Disable the internal open-drain of PC1 pin.
    = 1, Enable the internal open-drain of PC1 pin.
  * Bit 2 (ODC2) : = 0, Disable the internal open-drain of PC2 pin.
    = 1, Enable the internal open-drain of PC2 pin.
  * Bit 3 (ODC3) : = 0, Disable the internal open-drain of PC3 pin.
    = 1, Enable the internal open-drain of PC3 pin.
  * Bit 4 (ODC4) : = 0, Disable the internal open-drain of PC4 pin.
    = 1, Enable the internal open-drain of PC4 pin.
  * Bit 5 (ODC5) : = 0, Disable the internal open-drain of PC5 pin.
    = 1, Enable the internal open-drain of PC5 pin.
  * Bit 6 (ODC6) : = 0, Disable the internal open-drain of PC6 pin.
    = 1, Enable the internal open-drain of PC6 pin.
  * Bit 7 (ODC7) : = 0, Disable the internal open-drain of PC7 pin.
    = 1, Enable the internal open-drain of PC7 pin.

- **PortD Control Register: RC**

The RC register is both readable and writable.

* Bit 0 (IOPD0) : = 0, The PD0 pin is output mode.
  = 1, The PD0 pin is input mode.
* Bit 1 (IOPD1) : = 0, The PD1 pin is output mode.
  = 1, The PD1 pin is input mode.
* Bit 2 (/PHD0) : = 0, Enable the internal pull-high of PD0 pin.
  = 1, Disable the internal pull-high of PD0 pin.
* Bit 3 (/PHD1) : = 0, Enable the internal pull-high of PD1 pin.
  = 1, Disable the internal pull-high of PD1 pin.
* Bit 4 (/PDD0) : = 0, Enable the internal pull-down of PD0 pin.
  = 1, Disable the internal pull-down of PD0 pin.
* Bit 5 (/PDD1) : = 0, Enable the internal pull-down of PD1 pin.
  = 1, Disable the internal pull-down of PD1 pin.
* Bit 6 (ODD0) : = 0, Disable the internal open-drain of PD0 pin.
  = 1, Enable the internal open-drain of PD0 pin.
* Bit 7 (ODD1) : = 0, Disable the internal open-drain of PD1 pin.
  = 1, Enable the internal open-drain of PD1 pin.

- **Interrupt Status Register: RF**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1IF	WDTIF	T2IF			EXIF	PBIF	T0IF

* Bit 0 (T0IF) : Timer0 overflow interrupt flag. Set “1” when the Timer0 overflow, reset by software.
* Bit 1 (PBIF) : PortB input change interrupt flag. Set “1” when PortB input change, reset by software.
* Bit 2 (EXIF) : External INT pin interrupt flag. Set “1” when External INT pin interrupt, reset by software.
* Bit 3 ~ 4 : Not used.
* Bit 5 (T2IF) : Timer2 underflow interrupt flag. Set “1” when the Timer1 underflow, reset by software.
* Bit 6 (WDTIF) : Watchdog timer out interrupt flag. Set “1” when watchdog time out interrupt, reset by software.
* Bit 7 (T1IF) : Timer1 underflow interrupt flag. Set “1” when the Timer1 underflow, reset by software.

- **R10 ~ R1F , R20 ~ R3F**

R10 ~ R1F, R20 ~ R3F (Bank 0 ~ Bank3) are general storage registers.

- **T0MODE REGISTER**

T0MODE is a readable / writable register and the content is listed in following Table.

Bit	Symbol	Description			
		Bit value	Timer rate	WDT reset rate	WDT INT rate
2-0	PS2:PS0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256
3	PSC	Prescaler assign bit: = 0, Timer0 = 1, WDT			
4	TE	Timer0 source signal edge select bit: = 0, Increment when low-to-high transition on RTCC0 pin for TIM0 = 1, Increment when high-to-low transition on RTCC0 pin for TIM0			
5	TS	Timer0 source signal select bit: = 0, Internal instruction clock cycle = 1, Transition on RTCC0 pin			
6	INTF	Interrupt enable flag (Read Only) = 0, masked by DISI or hardware interrupt = 1, enabled by ENI / RETIE instructions			
7	INTEDG	Interrupt edge select bit = 0, interrupt on falling edge of INT pin = 1, interrupt on rising edge of INT pin			

* The first WDT Interrupt is 1/2 period after executing Reset function or CLRWDT instruction when the Prescaler is assigned to Watch Dog Timer.

3.2 I/O Control Registers (Addressed by IOST, IOSTR instruction)

- **Control PortA I/O Mode Register: F5 (PortA)**

The F5 register is both readable and writable.

= 0, the relative I/O pin is in output mode.

= 1, the relative I/O pin is in input mode.

- **Control PortB I/O Mode Register: F6 (PortB)**

The F6 register is both readable and writable.

= 0, the relative I/O pin is in output mode.

= 1, the relative I/O pin is in input mode.

- **Control PortC I/O Mode Register: F7 (PortC)**

The F7 register is both readable and writable.

= 0, the relative I/O pin is in output mode.

= 1, the relative I/O pin is in input mode.

- **PA4~PA7 Control Register: F8**

  The F8 register is both readable and writable.

  * Bit 0 (/PHA4) : = 0, Enable the internal pull-high of PA4 pin.
    = 1, Disable the internal pull-high of PA4 pin.
  * Bit 1 (/PHA6) : = 0, Enable the internal pull-high of PA6 pin.
    = 1, Disable the internal pull-high of PA6 pin.
  * Bit 2 (/PHA7) : = 0, Enable the internal pull-high of PA7 pin.
    = 1, Disable the internal pull-high of PA7 pin.
  * Bit 3 (/PDA5) : = 0, Enable the internal pull-down of PA5 pin.
    = 1, Disable the internal pull-down of PA5 pin.

- **PortB Input Change Interrupt Control Register: F9**

  The F9 register is both readable and writable.

  * Bit 0 (PBEI0) : = 0, Disable the input change interrupt function of PB0 pin.
    = 1, Enable the input change interrupt function of PB0 pin.
  * Bit 1 (PBEI1) : = 0, Disable the input change interrupt function of PB1 pin.
    = 1, Enable the input change interrupt function of PB1 pin.
  * Bit 2 (PBEI2) : = 0, Disable the input change interrupt function of PB2 pin.
    = 1, Enable the input change interrupt function of PB2 pin.
  * Bit 3 (PBEI3) : = 0, Disable the input change interrupt function of PB3 pin.
    = 1, Enable the input change interrupt function of PB3 pin.
  * Bit 4 (PBEI4) : = 0, Disable the input change interrupt function of PB4 pin.
    = 1, Enable the input change interrupt function of PB4 pin.
  * Bit 5 (PBEI5) : = 0, Disable the input change interrupt function of PB5 pin.
    = 1, Enable the input change interrupt function of PB5 pin.
  * Bit 6 (PBEI6) : = 0, Disable the input change interrupt function of PB6 pin.
    = 1, Enable the input change interrupt function of PB6 pin.
  * Bit 7 (PBEI7) : = 0, Disable the input change interrupt function of PB7 pin.
    = 1, Enable the input change interrupt function of PB7 pin.

- **Prescaler of Timer0 and WDT Counter Register: FA**

  The FA register is readable.

  The content of FA is the value of Prescaler Counter.

- **Pull Down Control Register: FB**

  The FB register is both readable and writable.

  * Bit 0 (/PDA0) : = 0, Enable the internal pull-down of PA0 pin.
    =1, Disable the internal pull-down of PA0 pin.

* Bit 1 (/PDA1) : = 0, Enable the internal pull-down of PA1 pin.
  =1, Disable the internal pull-down of PA1 pin.
* Bit 2 (/PDA2) : = 0, Enable the internal pull-down of PA2 pin.
  =1, Disable the internal pull-down of PA2 pin.
* Bit 3 (/PDA3) : = 0, Enable the internal pull-down of PA3 pin.
  =1, Disable the internal pull-down of PA3 pin.
* Bit 4 (/PDB0) : = 0, Enable the internal pull-down of PB0 pin.
  =1, Disable the internal pull-down of PB0 pin.
* Bit 5 (/PDB1) : = 0, Enable the internal pull-down of PB1 pin.
  =1, Disable the internal pull-down of PB1 pin.
* Bit 6 (/PDB2) : = 0, Enable the internal pull-down of PB2 pin.
  =1, Disable the internal pull-down of PB2 pin.
* Bit 7 (/PDB3) : = 0, Enable the internal pull-down of PB3 pin.
  =1, Disable the internal pull-down of PB3 pin.

- **PortB Open Drain Control Register: FC**

The FC register is both readable and writable.

* Bit 0 (ODB0) : = 0, Disable the internal open-drain of PB0 pin.
  = 1, Enable the internal open-drain of PB0 pin.
* Bit 1 (ODB1) : = 0, Disable the internal open-drain of PB1 pin.
  = 1, Enable the internal open-drain of PB1 pin.
* Bit 2 (ODB2) : = 0, Disable the internal open-drain of PB2 pin.
  = 1, Enable the internal open-drain of PB2 pin.
* Bit 3 (ODB3) : = 0, Disable the internal open-drain of PB3 pin.
  = 1, Enable the internal open-drain of PB3 pin.
* Bit 4 (ODB4) : = 0, Disable the internal open-drain of PB4 pin.
  = 1, Enable the internal open-drain of PB4 pin.
* Bit 5 (ODB5) : = 0, Disable the internal open-drain of PB5 pin.
  = 1, Enable the internal open-drain of PB5 pin.
* Bit 6 (ODB6) : = 0, Disable the internal open-drain of PB6 pin.
  = 1, Enable the internal open-drain of PB6 pin.
* Bit 7 (ODB7) : = 0, Disable the internal open-drain of PB7 pin.
  = 1, Enable the internal open-drain of PB7 pin.

- **PortB Pull High Control Register: FD**

The FD register is both readable and writable.

* Bit 0 (/PHB0) : = 0, Enable the internal pull-high of PB0 pin.
  = 1, Disable the internal pull-high of PB0 pin.

* Bit 1 (/PHB1) : = 0, Enable the internal pull-high of PB1 pin.
= 1, Disable the internal pull-high of PB1 pin.
* Bit 2 (/PHB2) : = 0, Enable the internal pull-high of PB2 pin.
= 1, Disable the internal pull-high of PB2 pin.
* Bit 3 (/PHB3) : = 0, Enable the internal pull-high of PB3 pin.
= 1, Disable the internal pull-high of PB3 pin.
* Bit 4 (/PHB4) : = 0, Enable the internal pull-high of PB4 pin.
= 1, Disable the internal pull-high of PB4 pin.
* Bit 5 (/PHB5) : = 0, Enable the internal pull-high of PB5 pin.
= 1, Disable the internal pull-high of PB5 pin.
* Bit 6 (/PHB6) : = 0, Enable the internal pull-high of PB6 pin.
= 1, Disable the internal pull-high of PB6 pin.
* Bit 7 (/PHB7) : = 0, Enable the internal pull-high of PB7 pin.
= 1, Disable the internal pull-high of PB7 pin

- **System Control Register: FE**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	LVRE	ROC	LPRE	CONC		

The FE register is both readable and writable.

* Bit 0~1 : Not used.
* Bit 2 (CONC) = 1, Enable Constant Sink Current Mode of PB1/IR pin.
PB1/IR Pin will provide constant output-low-sink current about 40mA when PB1/IR pin is configured as output mode.
= 0, Disable Constant Sink Current Mode of PB1/IR pin.
* Bit 3 (LPRE) = 1, Enable Low Power reset
= 0, Disable Low Power reset
* Bit 4 (ROC) = 1, Enable R-option function of PA0 and PA1 pin.If a external resistor 430KΩ is connected / disconnected to VSS on PA0 (PA1) pin, the status of PA0 (PA1) is read as “0” / “1”.
= 0, Disable R-option function of PA0 and PA1 pin.
* Bit 5 (LVRE) = 1, Enable low voltage reset.(Precise Low voltage reset selection by configuration word)
= 0, Disable low voltage reset.(Precise Low voltage reset selection by configuration word)
* Bit 6 (EIS) = 1, External interrupt pin is selected. The I/O control bit of PD1 (bit 1 of RC register) must be set to “1”, the status of INT pin can be read by reading PortD.
= 0, PD1 is bi-directional I/O pin.
* Bit 7 (WDTE) = 1, Enable Watchdog timer.
= 0, Disable Watchdog timer.

- **Interrupt Mask Register: FF**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1IE	WDTIE	T2IE			EXIE	PBIE	T0IE

The FF register is both readable and writable.

* Bit 0 (T0IE) : = 1, Enable the Timer0 overflow interrupt.
  = 0, Disable the Timer0 overflow interrupt.

* Bit 1 (PBIE) : = 1, Enable the PortB input change interrupt.
  = 0, Disable the PortB input change interrupt.

* Bit 2 (EXIE) : = 1, Enable the External INT pin interrupt.
  = 0, Disable the External INT pin interrupt.

* Bit 3 ~ 4 : Not used.

* Bit 5 (T2IE) : = 1, Enable the Timer2 underflow interrupt.
  = 0, Disable the Timer2 underflow interrup.

* Bit 6 (WDTIE) : If the watchdog interrupt function is enabled by programming configuration word,
  = 1, Enable watchdog interrupt.
  = 0, Disable watchdog interrupt.

* Bit 7 (T1IE) : = 1, Enable the Timer1 underflow interrupt.
  = 0, Disable the Timer1 underflow interrup.

3.3 Special Function Registers (Addressed by SFUN, SFUNR instruction)

8 bit Reload Down-Counter Timer1:

- **Timer1 Initial/reload register: S0**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

* The S0 register is both readable and writable.

* Write: The initial/reload value.

* Read: The counter value.

- **Timer1 control register1: S1**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0:disable PWM1 output 1:enable PWM1 output	PWM1 output 0: Active High 1: Active Low				1:One-shot mode 0:Non-Stop mode	1:re-load mode 0:continuous mode	1:Start count 0:Stop count
W	W				R/W	R/W	R/W

* Re-load mode: The counter will load the initial value into the counter while counter underflows.

* Continuous mode: The counter will keep counting from FF while counter underflows.

* Non-stop mode: The counter will keep counting even counter underflows.

* One-shot mode: The counter will stop while counter underflows.

* The re-load / Continuous function is meaningful only in Non-stop mode.

* When Bit 7 is set "1", then the PB6/PWM1 pin will be switch to PWM1 output.

* Notice: Always stop the counter then write initial value.

- **Timer1 control register2: S2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Timer1 clock source selection (T1S) 0:Internal instruction cycle clock 1:RTCC0 pin	RTCC0 pin signal edge select (T1E)	Prescaler1 function (PS1ENB) 0: enable 1: disable	Prescale rate selection bits (PS1_2 : PS1_0) 000: 1:2 001: 1:4 010: 1:8 011: 1:16 100: 1:32 101: 1:64 110: 1:128 111: 1:256		

* The S2 register is both readable and writable.

* Bit 4: =1, "Decrement counting" when high-to-low transition on RTCC0 pin for Timer1.

=0, "Decrement counting" when low-to-high transition on RTCC0 pin for Timer1.

* The Prescaler1's output is the Timer1's clock source when Prescaler1 function is enabled.

- **PWM1 register: S3**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

* The S3 register is only writable.

* Under PWM1 output is set "Active High" in Timer1 Control Register1, every time the Timer1 enable or underflow, PWM1 output will be set as low until the TIMER1's value equals to the PWM1 value then setting to high; When PWM1 output is set "Active Low" in Timer1 Control Register1 is the opposite.

* The Timer1's re-load value adjusts the output frequency and the PWM1 register defines the output waveform's duty.

- **Prescaler1 of Timer1 Counter Register: S4**

* The S4 register is readable.

* The content of S4 is the value of Prescaler1 Counter.

- **Buzzer1 control register: S5**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0:disable Buzzer1 output 1:enable Buzzer 1 output				Frequency selection of Buzzer1 output (BZ1S3 : BZ1S0) 0000: Clock source frequency of Prescaler1 / 2 0001: Clock source frequency of Prescaler1 / 4 0010: Clock source frequency of Prescaler1 / 8 0011: Clock source frequency of Prescaler1 / 16 0100: Clock source frequency of Prescaler1 / 32 0101: Clock source frequency of Prescaler1 / 64 0110: Clock source frequency of Prescaler1/ 128 0111: Clock source frequency of Prescaler1 / 256 1000: Clock source frequency of Timer1 / 2 1001: Clock source frequency of Timer1 / 4 1010: Clock source frequency of Timer1 / 8 1011: Clock source frequency of Timer1 / 16 1100: Clock source frequency of Timer1 / 32 1101: Clock source frequency of Timer1 / 64 1110: Clock source frequency of Timer1 / 128 1111: Clock source frequency of Timer1 / 256			
W				W			

* The S5 register is only writable.

* When Bit 7 is set "1", then the PB7/BZ1 pin will be switch to Buzzer1 output.

FIGURE 3.1: Block Diagram of Timer1, Buzzer1 and PWM1

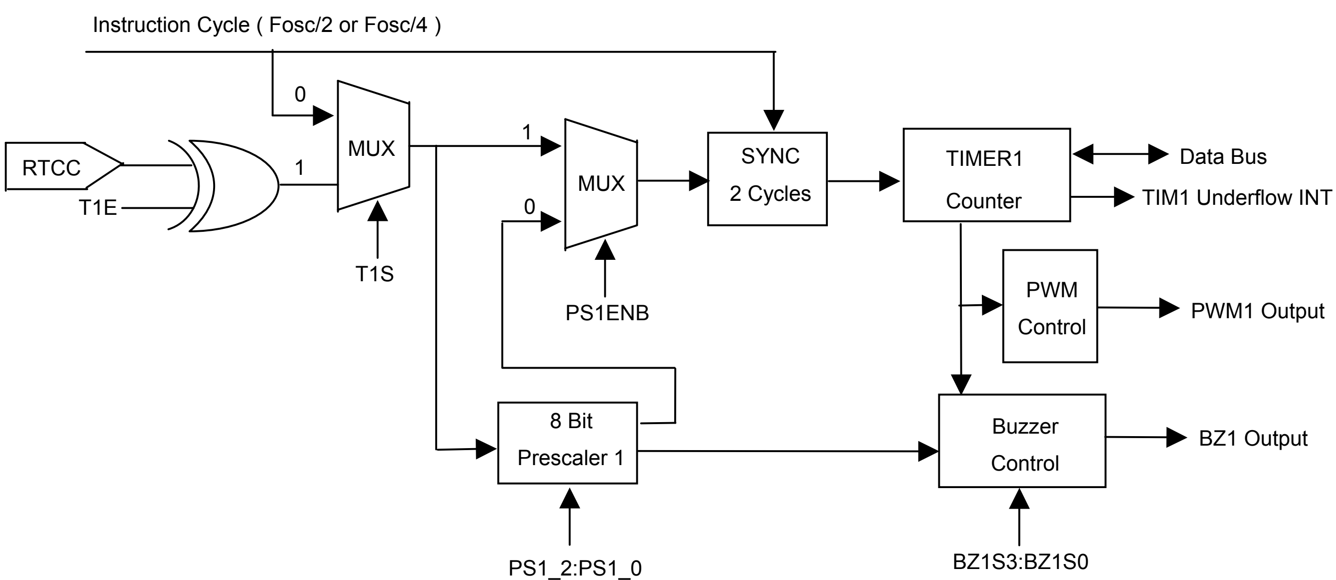
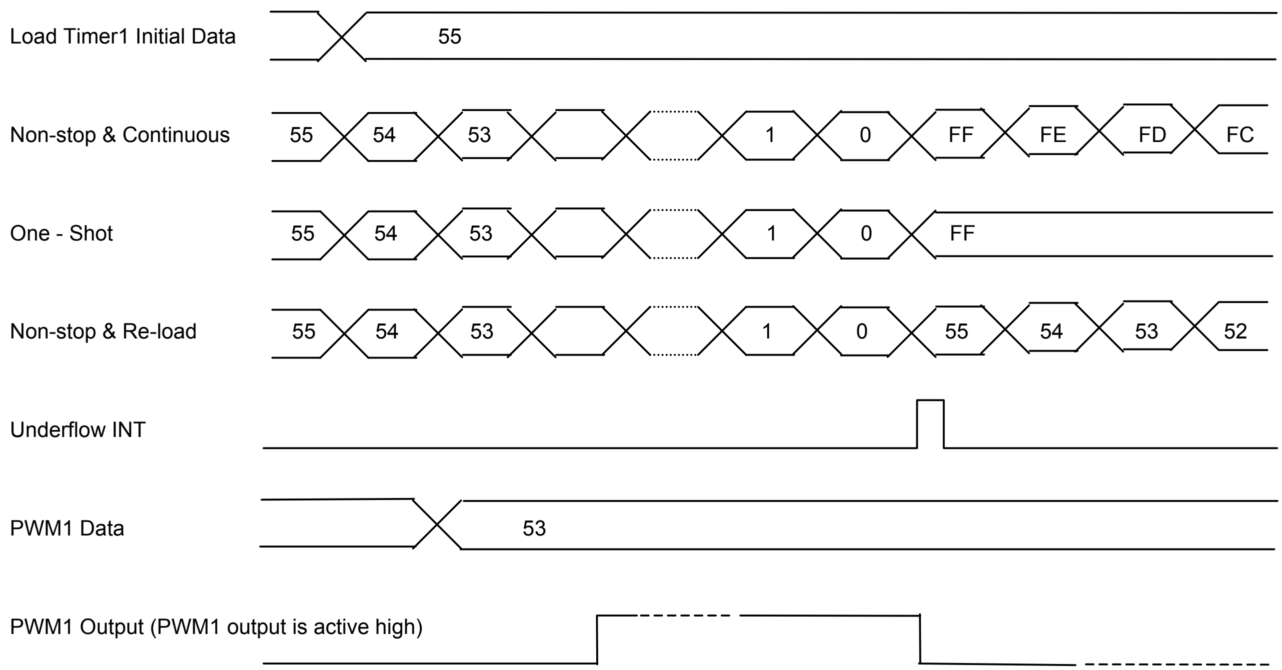


FIGURE 3.2: Timing Chart of Timer1 and PWM1



- **IR Control register: S6**

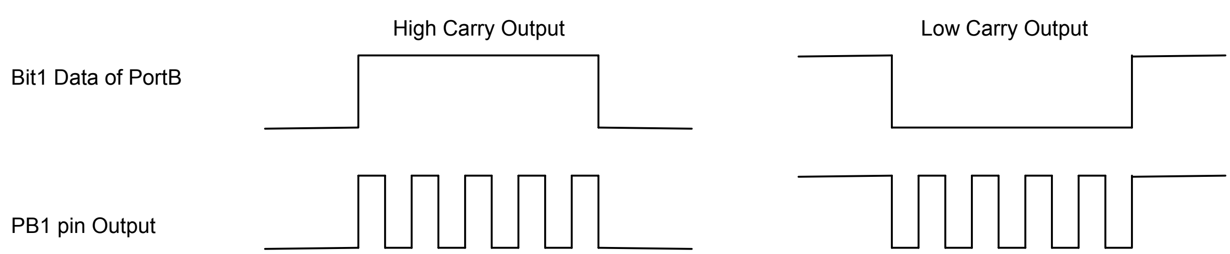
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IR Clock(Fosc) Input Frequency Selection 0: 455KHz 1: 3.58MHz					0:High Carry output 1:Low Carry output	IR Output Frequency Secection 0: 38K Hz 1: 57K Hz	IR function 0:disable 1:enable

* The S6 register is only writable.

* If Bit0 is set "1" to enable IR function, the PB1/IR pin will be auto configured to output mode and output the data of PortB bit1 in IR function mode.

* The "High Carry Output " means to output high data with IR carry to PB1/IR pin and the "Low Carry Output " is the opposite.

FIGURE 3.3: Timing Chart of IR Carry Output



- **Table High-Order Byte Pointer register (TBHP): S7**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					D2	D1	D0

* The S7 register is both readable and writable.

* The content of TBHP will associate with ACC to be loaded into PC bits< 10:0 > when program executes CALLA or GOTOA instruction. Additionally, the TBHP register is used for high part address to access ROM code data in executing the TABLE instruction.

- **Table High-Order Byte Data register (TBH): S8**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		D5	D4	D3	D2	D1	D0

* The S8 register is only readable.

* Move the high byte of the addressed ROM code to TBH register by TABLE instruction.

8 bit Reload Down-Counter Timer2:

- **Timer2 Initial/reload register: S9**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

* The S9 register is both readable and writable.

* Write: The initial/reload value.

* Read: The counter value.

- **Timer2 control register1: SA**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0:disable PWM2 output 1:enable PWM2 output	PWM2 output 0: Active High 1: Active Low				1:One-shot mode 0:Non-Stop mode	1:re-load mode 0:continuous mode	1:Start count 0:Stop count
W	W				R/W	R/W	R/W

* Re-load mode: The counter will load the initial value into the counter while counter underflows.

* Continuous mode: The counter will keep counting from FF while counter underflows.

* Non-stop mode: The counter will keep counting even counter underflows.

* One-shot mode: The counter will stop while counter underflows.

* The re-load / Continuous function is meaningful only in Non-stop mode.

* When Bit 7 is set “1”, then the PC0/PWM2 pin will be switch to PWM2 output.

Notice: Always stop the counter then write initial value.

- **Timer2 control register2: SB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Timer2 clock source selection (T2S) 0:Internal instruction cycle clock 1:RTCC1 pin	RTCC1 pin signal edge select (T2E)	Prescaler2 function (PS2ENB) 0: enable 1: disable	Prescale rate selection bits (PS2_2 : PS2_0) 000: 1:2 001: 1:4 010: 1:8 011: 1:16 100: 1:32 101: 1:64 110: 1:128 111: 1:256		

* The SB register is both readable and writable.

* Bit 4: =1, "Decrement counting" when high-to-low transition on RTCC1 pin for Timer2.

=0, "Decrement counting" when low-to-high transition on RTCC1 pin for Timer2.

* The Prescaler2's output is the Timer2's clock source when Prescaler2 function is enabled.

- **PWM2 register: SC**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

* The SC register is only writable.

* Under PWM2 output is set "Active High" in Timer2 Control Register1, every time the Timer2 enable or underflow, PWM2 output will be set as low until the TIMER2's value equals to the PWM2 value then setting to high; When PWM2 output is set "Active Low" in Timer2 Control Register1 is the opposite.

* The Timer2's re-load value adjusts the output frequency and the PWM2 register defines the output waveform's duty.

- **Prescaler2 of Timer2 Counter Register: SD**

* The SD register is readable.

* The content of SD is the value of Prescaler2 Counter.

- **Buzzer2 control register: SE**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0:disable Buzzer2 output 1:enable Buzzer2 output				Frequency selection of Buzzer output (BZ2S3 : BZ2S0) 0000: Clock source frequency of Prescaler2 / 2 0001: Clock source frequency of Prescaler2 / 4 0010: Clock source frequency of Prescaler2 / 8 0011: Clock source frequency of Prescaler2 / 16 0100: Clock source frequency of Prescaler2 / 32 0101: Clock source frequency of Prescaler2 / 64 0110: Clock source frequency of Prescaler2/ 128 0111: Clock source frequency of Prescaler2 / 256 1000: Clock source frequency of Timer2 / 2 1001: Clock source frequency of Timer2 / 4 1010: Clock source frequency of Timer2 / 8 1011: Clock source frequency of Timer2 / 16 1100: Clock source frequency of Timer2 / 32 1101: Clock source frequency of Timer2 / 64 1110: Clock source frequency of Timer2 / 128 1111: Clock source frequency of Timer2 / 256			
W				W			

* The SE register is only writable.

* When Bit 7 is set “1”, then the PC1/BZ2 pin will be switch to buzzer2 output.

FIGURE 3.4: Block Diagram of Timer2, Buzzer2 and PWM2

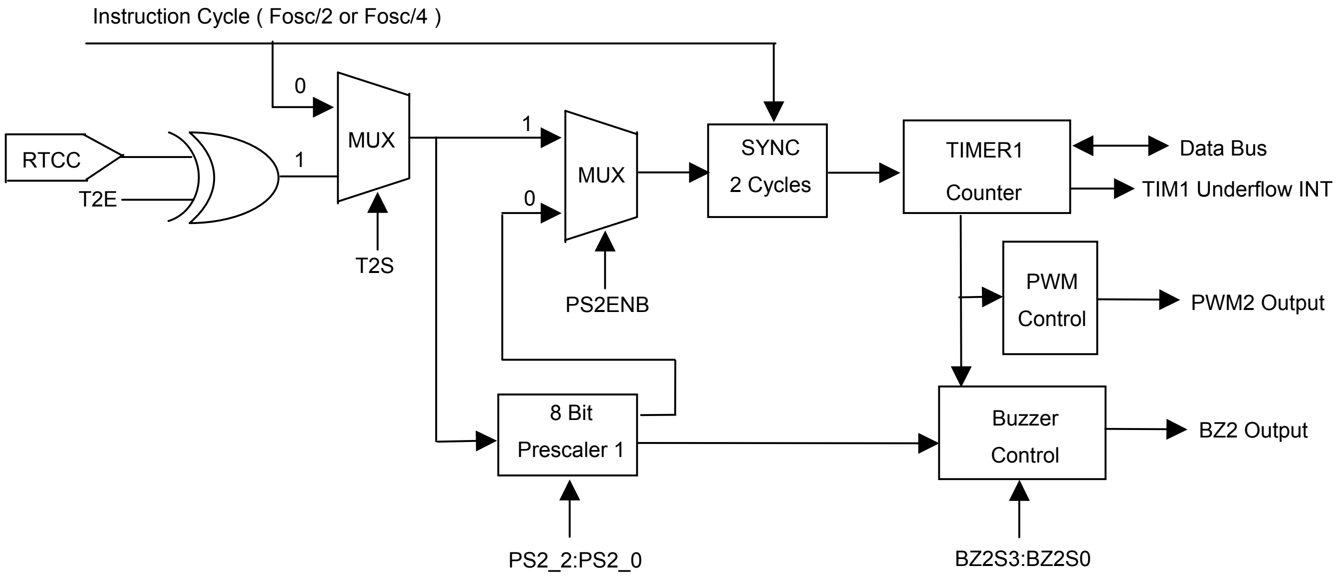
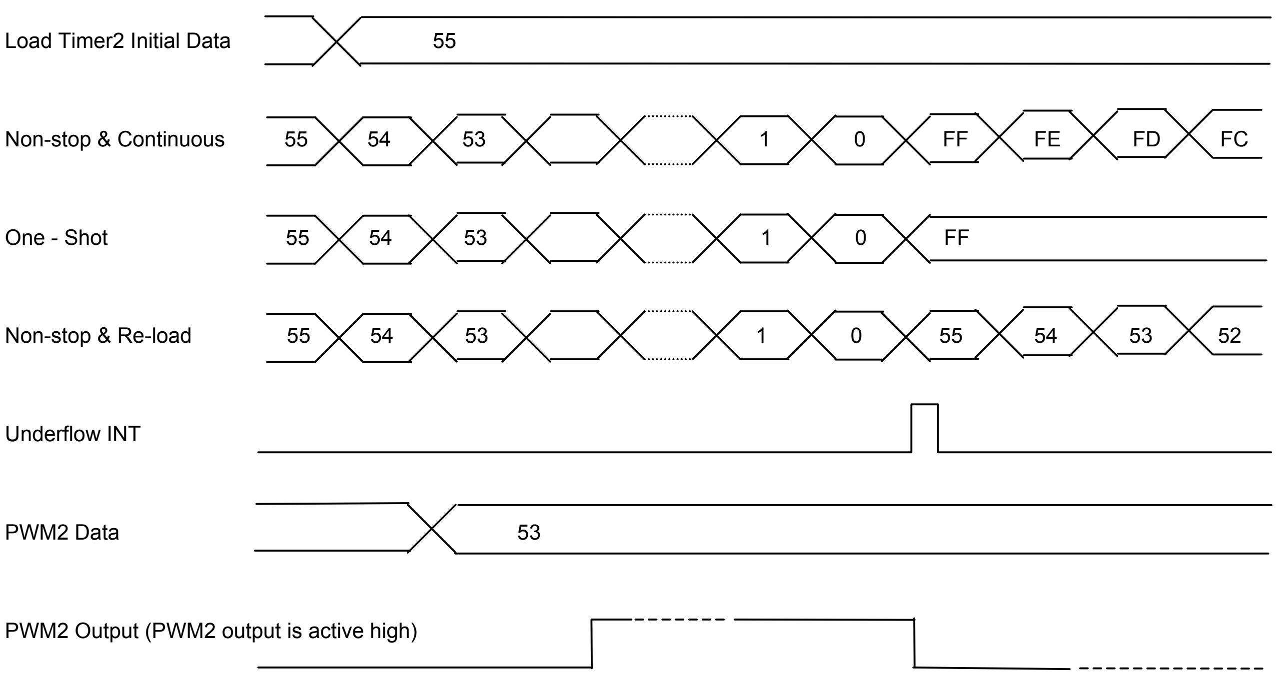


FIGURE 3.5: Timing Chart of Timer2 and PWM2



3.4 RESET

This device may be reset in one of the following events:

(1) Power-on reset: At power-up, this device will be kept in a reset condition until the power voltage on Reset pin has reached a logic high level.

(2) Reset pin is “LOW” state input. (if Reset pin is configured as reset function.)

(3) WDT time-out reset (if WDT is enabled and WDT reset function is enabled.)

(4) Low voltage reset (if Low voltage function is enabled.)

The contents of registers after reset are listed below:

Address	Register	Power-On Reset	Reset or WDT Reset
00h	INAR	xxxx xxxx	uuuu uuuu
01h	Timer0	xxxx xxxx	uuuu uuuu
02h	PCL	0000 0000	0000 0000
03h	STATUS	0001 1xxx	000# #uuu
04h	FSR	00xx xxxx	00 uu uuuu
05h	PortA	xxxx xxxx	uuuu uuuu
06h	PortB	xxxx xxxx	uuuu uuuu
07h	PortC	xxxx xxxx	uuuu uuuu
08h	PortD	---- --xx	---- --uu
09h	PortC Pull High Control Register	1111 1111	1111 1111
0Ah	PortC Pull Down Control Register	1111 1111	1111 1111
0Bh	PortC Open Drain Control Register	0000 0000	0000 0000
0Ch	PortD Control Register	0011 1111	0011 1111
0Fh	Interrupt Status Register	000- -000	000- -000
10h-1Fh	General Storage Register	xxxx xxxx	uuuu uuuu
20h-3Fh	General Storage Register (Bank0 ~ Bank3)	xxxx xxxx	uuuu uuuu
N/A	ACC	xxxx xxxx	uuuu uuuu
N/A	T0MODE	0011 1111	0011 1111
N/A	Control PortA I/O Reg (F5)	1111 1111	1111 1111
N/A	Control PortB I/O Reg (F6)	1111 1111	1111 1111
N/A	Control PortC I/O Reg (F7)	1111 1111	1111 1111
N/A	PA4 ~ PA7 Control Register (F8)	---- 1111	---- 1111
N/A	PortB Input Change Interrupt Control Register (F9)	1111 1111	1111 1111
N/A	Prescaler of Timer0 and WDT Register(FA)	1111 1111	1111 1111
N/A	Pull Down Control Register (FB)	1111 1111	1111 1111
N/A	PortB Open Drain Control Register (FC)	0000 0000	0000 0000
N/A	PortB Pull High Control Register (FD)	1111 1111	1111 1111
N/A	System Control Register(FE)	1010 00--	1010 00--
N/A	Interrupt Mask Register (FF)	000- -000	000- -000
N/A	Timer1 Initial/reload register(S0)	xxxx xxxx	uuuu uuuu
N/A	Timer1 control register1 (S1)	00-- -000	00-- -000
N/A	Timer1 control register2 (S2)	--11 1111	--11 1111
N/A	PWM1 register(S3)	xxxx xxxx	uuuu uuuu
N/A	Prescaler1 of Timer1 Counter Register(S4)	1111 1111	1111 1111
N/A	Buzzer1 Control Register(S5)	0--- 1111	0--- 1111
N/A	IR Control register(S6)	0--- -000	0--- -000

Address	Register	Power-On Reset	Reset or WDT Reset
N/A	Table High-Order Byte Pointer register (S7)	---- -xxx	---- -uuu
N/A	Table High-Order Byte Data register (S8):	--xx xxxx	--uu uuuu
N/A	Timer2 Initial/reload register(S9)	xxxx xxxx	uuuu uuuu
N/A	Timer2 control register1 (SA)	00-- -000	00-- -000
N/A	Timer2 control register2 (SB)	--11 1111	--11 1111
N/A	PWM2 register(SC)	xxxx xxxx	uuuu uuuu
N/A	Prescaler2 of Timer2 Counter Register(SD)	1111 1111	1111 1111
N/A	Buzzer2 Control Register(SE)	0--- 1111	0--- 1111

Note: x = unknown, u = unchanged, - = unimplemented, # = see the following table

TO/PD status after Reset:

Condition	Status: bit 4 TO	Status: bit 3 PD
Power-on Reset	1	1
Reset pin Reset (Non-SLEEP)	u	u
Reset pin Wake-up Reset or Interrupt Wake-up from SLEEP	1	0
WDT Reset (Non-SLEEP)	0	1
WDT Wake-up Reset from SLEEP	0	0

Note: u = unchanged

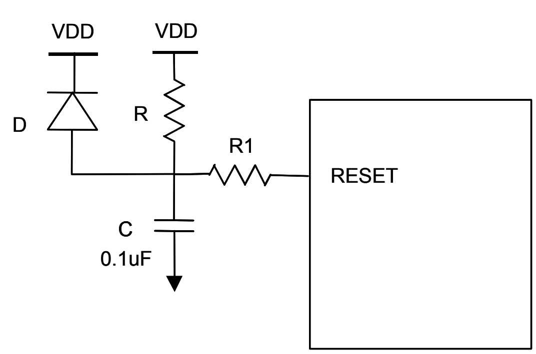
TO/PD status is affected by events:

Event	Status: bit 4 TO	Status: bit 3 PD
Power-on	1	1
SLEEP instruction	1	0
CLRWDT instruction	1	1
WDT Time-out when WDT reset is enabled	0	u

Note: u = unchanged

WDT wake-up from sleep mode: executing the SLEEP instruction can force this device entering into sleep mode (power saving mode). While system is in sleep mode, the WDT is cleared but keeps running. This device can be awakened by WDT time-out when WDT reset function is enabled or reset input on Reset pin.

The following figure is power-on reset circuit for slow VDD power-up:



- It is recommended the R value should be not greater than 40k ohms to make sure the voltage of RSET pin can meet specification.
- The R1 value = 100 ohms ~ 1K ohms will prevent high current, ESD or Electrical Overstress flowing into RESET pin.
- The diode helps discharge quickly when power down.

3.5 I/O Ports

The Port A and Port B are Bi-directional tri-state I/O ports. Both Port A and Port B are 8-pin I/O port. Bit13 of the Configuration Word will decide the Pin function of PA5/Reset. If this bit is set "1", the PA5/Reset Pin will be assigned to Reset function (Default) and forced as input; If this bit is cleared to "0", the PA5/Reset Pin will be assigned to digital I/O function.

The Bit[2:0] of the Configuration Word can select oscillator mode. Besides, these bits can decide the pin function of PA6 and PA7.

The I/O Mode Register F5(Port A) and F6(Port B) can configure these I/O pins as output or input. The PA4~PA7 Control Register F8 can control the internal pull-high or pull-down of PA4 ~ PA7. The Pull Down Control Register FB can enable corresponding internal pull-down of PB3 ~ PB0, PA3 ~ PA0. The Open Drain Control Register FC can enable open drain function of PB7 ~ PB0. The Pull High Control Register FD can enable internal pull-high of PB7 ~ PB0.

Setting PortB Input Change Interrupt Control Register F9 can enable input Status Change Interrupt/Wake-up function.

PD1 provide an external interrupt function by setting the EIS bit of the System Control Register FE.

PA1, PA0 are the R-option pins enabled by setting the ROC bit of the System Control Register FE. If an external resistor 430KΩ is connected / disconnected to VSS on PA0 (PA1) pin, the status of PA0 (PA1) is read as "0" / "1".

FIGURE 3.6: Port A0~Port A4, Port A6 and Port A7 Equivalent Circuit (Pull-down or Pull high is not shown in the figure)

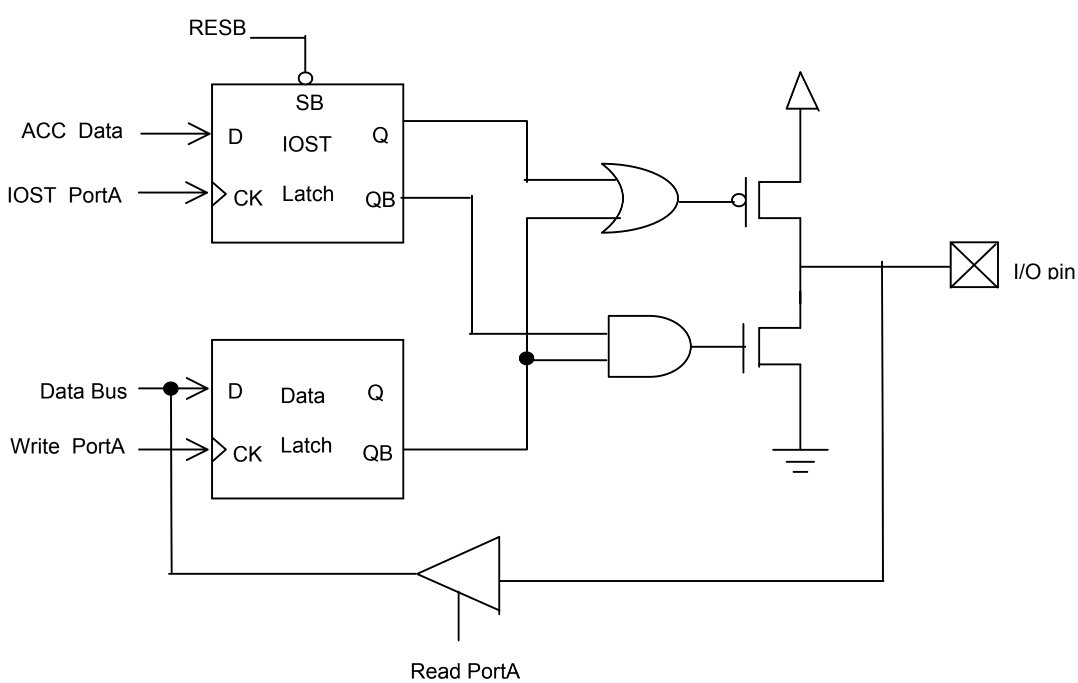


FIGURE 3.7: Port A5 Equivalent Circuit (Pull-down or Pull high is not shown in the figure)

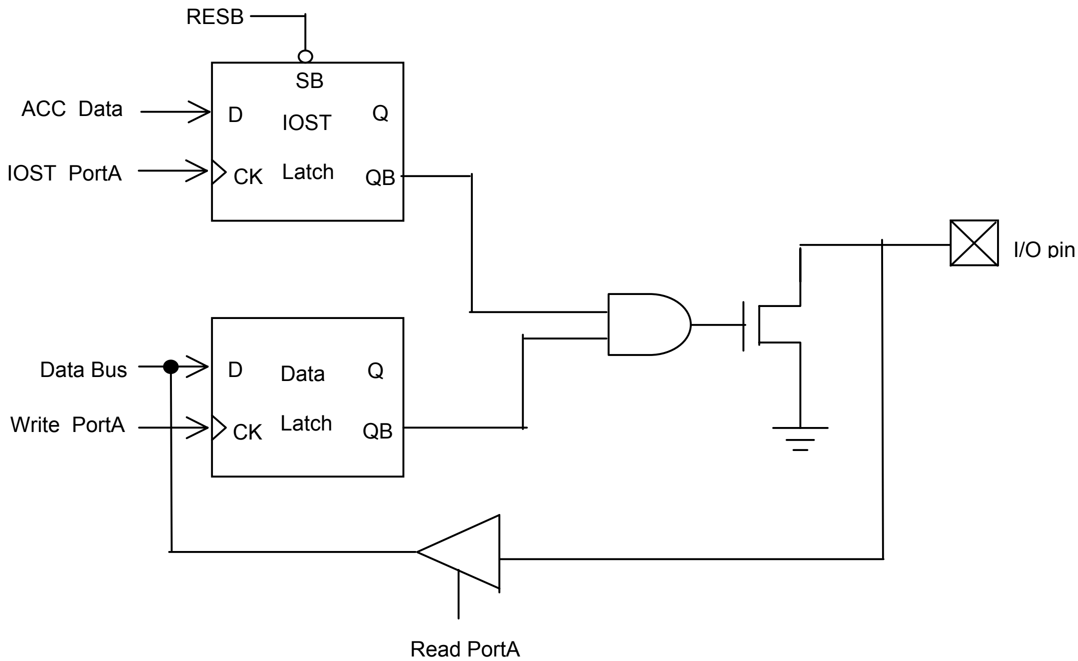


FIGURE 3.8: PB0 ~ PB7 Equivalent Circuit (Pull-down, pull-high and open-drain are not shown in the figure)

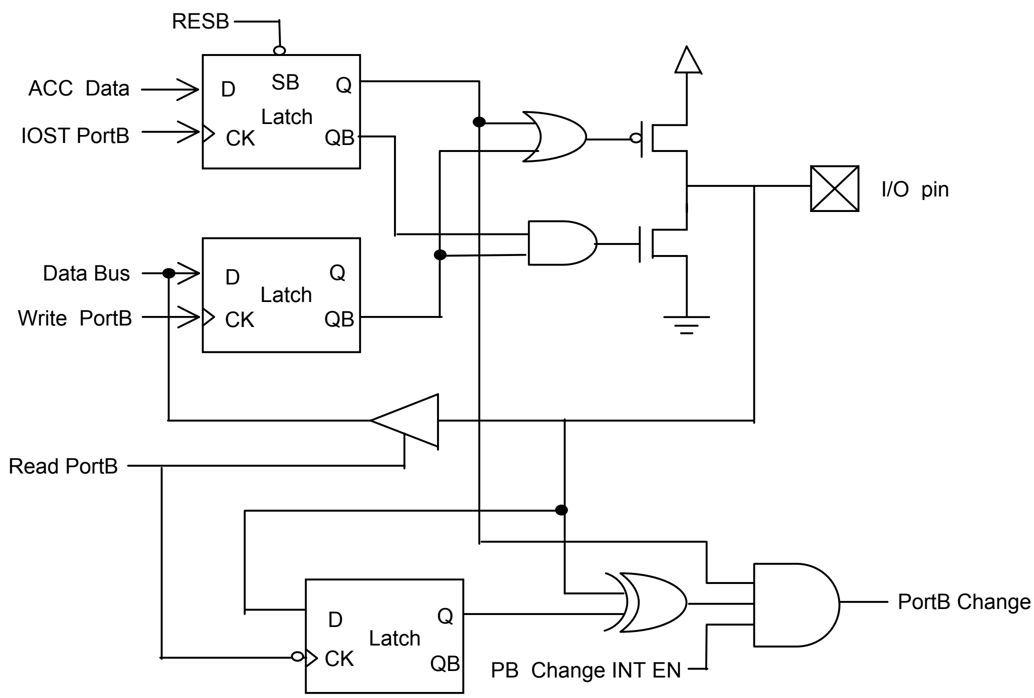
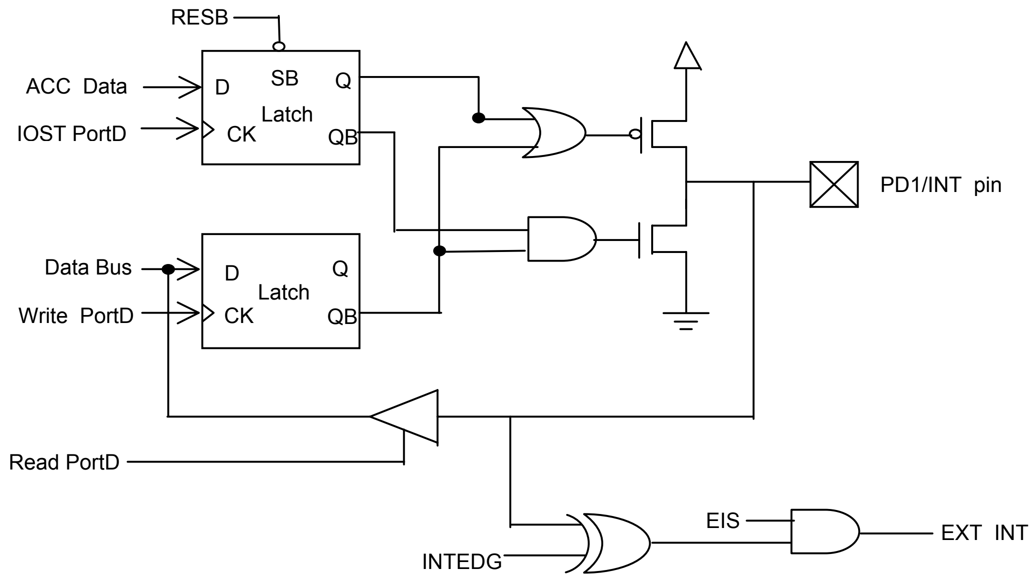


FIGURE 3.9: PD0/INT Equivalent Circuit (Pull-down, pull-high and open-drain are not shown in the figure)



3.6 Real Time Clock (TIMER0) And Watchdog Timer

3.6.1 Timer0

Timer0 is an 8-bit timer/counter. The clock source of Timer0 can be from the internal clock or by an external clock source presented at the RTCC0 pin.

To select the internal clock source, bit 5 of the T0MODE register should be reset. In this mode, Timer0 will increase by 1 in every instruction cycle (without prescaler).

To select the external clock source, bit 5 of the T0MODE register should be set. In this mode, Timer0 will increase by 1 on every falling edge or rising edge of RTCC0 pin is controlled by bit 4 of T0MODE register.

3.6.2 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator. This RC oscillator is separated from the RC oscillator of the OSCI pin. That means the WDT will keep running even when the oscillator driver is turned off, such as in sleep mode. During normal operation or in sleep mode, a WDT time-out will cause the device reset and the TO bit (bit 4 of STATUS register) will be cleared.

Without prescaler, the WDT time-out period is 18ms. This period can be increased by using the prescaler. The division ratio of prescaler is up to 1:128. Thus, the longest time-out period is approximately 2.3s.

3.6.3 Prescaler

The 8-bit prescaler may be assigned to either the Timer0 or the WDT through the PSC bit (bit 3 of the T0MODE register). Setting this bit assigns the prescaler to the WDT. Resetting this bit assigns the prescaler to the Timer0. The PS2:PS0 bits determine the prescale ratio. When assigned to Timer0, the prescaler will be cleared by instructions which write to Timer0 Register. A CLRWDT instruction will clear the WDT and prescaler when assigned to WDT. The prescaler can not be assigned to both the Timer0 and WDT simultaneously.

3.6.4 Switching Prescaler Assignment

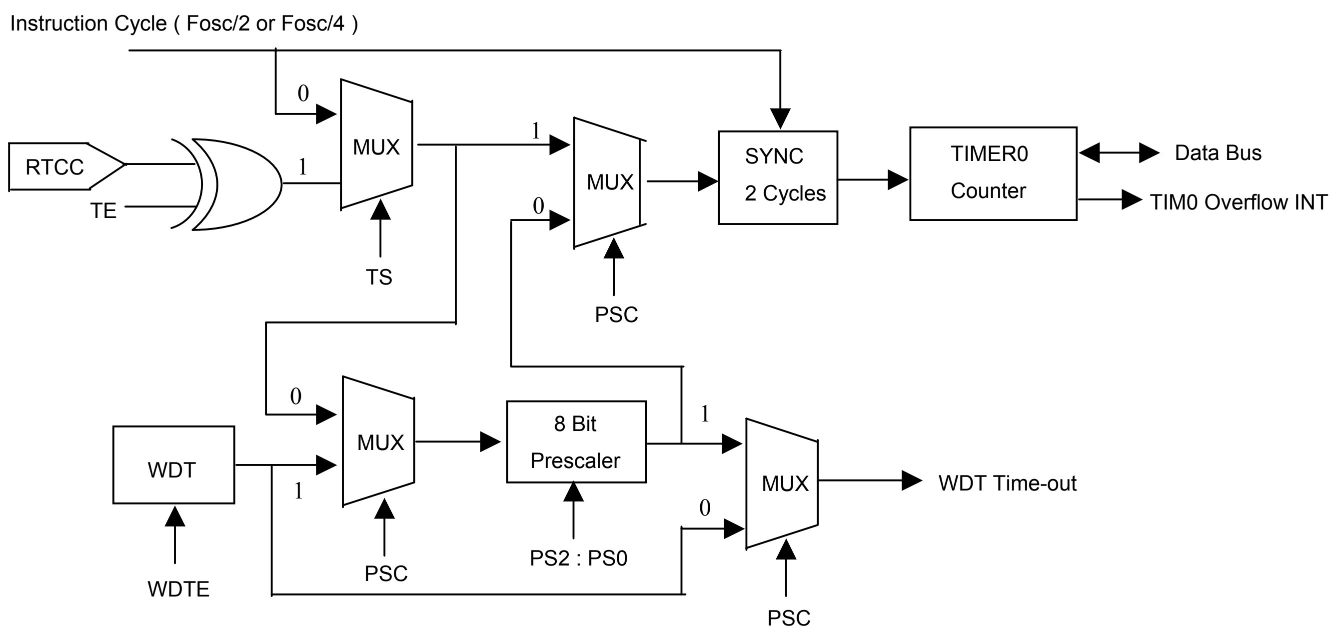
The prescaler switch can be assigned by software control. To avoid an unintended RESET, the following program rule must be observed when changing the prescaler assignment from Timer0 to WDT :

```
CLRWDT
MOVIA  b'xxxx1xxx'
CLRR   TIM0
T0MODE
```

A CLRWDT instruction should be executed before changing the prescaler assignment from WDT to Timer0 :

```
CLRWDT
MOVIA  b'xxxx0xxx'
T0MODE
```

FIGURE 3.10: Block Diagram of Timer0 and WDT



3.7 Oscillator Configuration

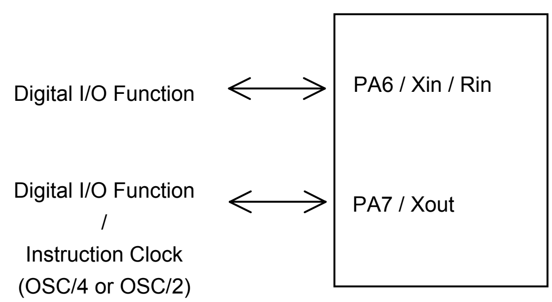
This device supports six oscillator modes. The user can program the three Bit[2:0] of configuration word to select appropriate mode. These oscillator modes offered as:

- IRC: Internal Resistor and Capacitor oscillator
- EXT-R: External Resistor and internal Capacitor oscillator
- LF-XTAL: Low frequency crystal oscillator
- XTAL: Standard crystal oscillator
- HF-XTAL: High frequency crystal oscillator
- ERC: External Resistor and Capacitor oscillator

3.7.1 IRC Mode

The Internal Resistor and Capacitor mode (IRC) can be enabled by setting Bit[2:0] of configuration word and program Bit[5:3] to select output frequency of internal oscillator.

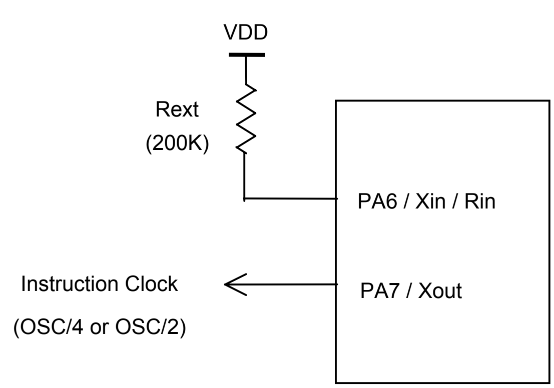
In IRC mode, PA6/Xin/Rin pin will be assigned to PA6 digital I/O, PA7/Xout pin will be assign to PA7 digital I/O or output instruction clock depend on the selection of configuration word Bit[2:0].



3.7.2 EXT-R Mode

In EXT-R mode adopts External resistor and internal capacitor to creat oscillator so PA6/Xin/Rin pin need to connect to Rext.By setting Bit[2:0] and Bit[5:3] of configuration word to enter EXT-R mode and select oscillator frequency. Resistance value of Rext can be tuned to produce more precise oscillator's frequency. The recommended value of Rext is 200K.

In EXT-R mode, PA7/Xout pin will output instruction clock.



3.7.3 LF-XTAL, XTAL, HF-XTAL Mode

AM8EB serial provide LF-XTAL, XTAL and HF-XTAL for different frequency crystal or ceramic oscillator. In these mode, a crystal or ceramic resonator is connected to Xin pin and Xout pin to create oscillation, refer to the specification of crystal or ceramic resonator to adopt appropriate C1, C2 or RS value.

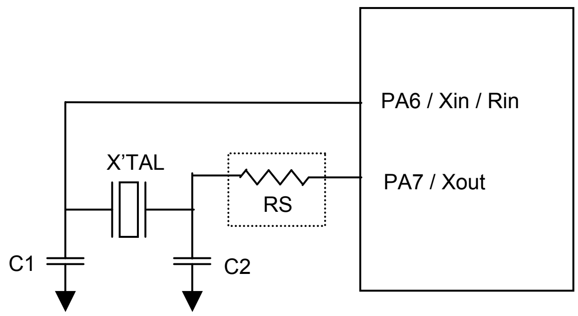
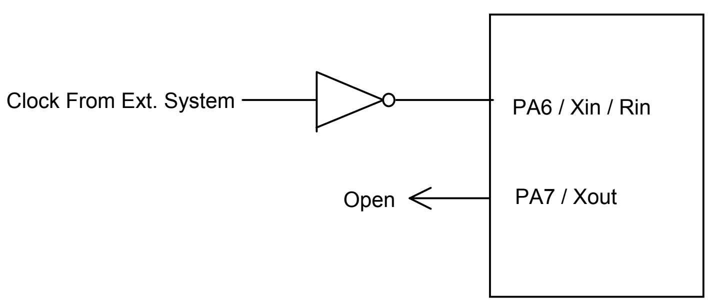


TABLE 3.2: Capacitor Value for Crystal (VDD = 3V)

Mode	Freq.	C1 (pF)	C2 (pF)
HF-XTAL	20 MHz	5 ~ 10	5 ~ 10
	16 MHz	5 ~ 10	5 ~ 10
	10 MHz	5 ~ 30	5 ~ 30
XTAL	8 MHz	5 ~ 20	5 ~ 20
	4 MHz	5 ~ 30	5 ~ 30
	1 MHz	5 ~ 30	5 ~ 30
	455 KHz	10 ~ 100	10 ~ 100
LF-XTAL	100 KHz	5 ~ 20	5 ~ 20
	32.768 KHz	5 ~ 30	5 ~ 30

In LF-XTAL, XTAL or HF-XTAL mode, the Xin pin can be driven directly by an external clock source.



3.7.4 ERC Mode

The oscillator frequency of External Resistor and Capacitor Oscillator mode (ERC) will be influenced by the value of Rext, Cext, the supply voltage and the working temperature. In addition to these, the frequency will slightly vary between different chip due to the variation of manufacturing process parameter.

In order to keep stable oscillator frequency, the value of Rext should be less than 1M ohm, the value of Cext should be greater than 20pF. In ERC mode, PA7/Xout pin will output instruction clock.

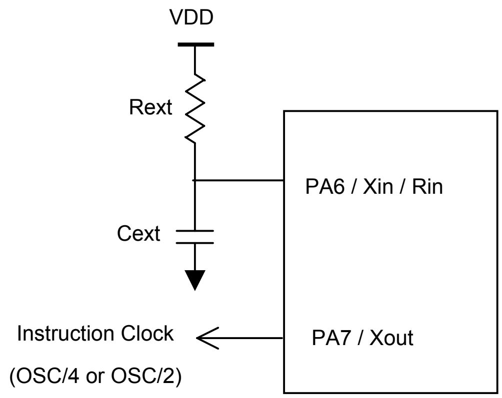


TABLE 3.3: ERC Oscillator Frequency Table

Cext	Rext	OSC @ 3V	OSC @ 5V
20 pF	3.3K	4.43 MHz	4.86 MHz
	5.1K	3.37 MHz	3.43 MHz
	10K	2.00 MHz	1.93 MHz
	100K	254.5 KHz	221.4 KHz
100 pF	3.3K	1.93 MHz	1.88 MHz
	5.1K	1.36 MHz	1.27 MHz
	10K	741.9 KHz	668.7 KHz
	100K	83.3 KHz	71.8 KHz
300 pF	3.3K	926 KHz	845 KHz
	5.1K	628 KHz	562 KHz
	10K	330 KHz	289 KHz
	100K	35 KHz	30 KHz

3.8 Interrupts

The AM8EB057A has six sources of interrupt:

- Timer0 overflow
- Timer1 underflow
- Timer2 underflow
- PB input change
- External Interrupt Pin
- Watchdog time out Interrupt (If the function is enabled by setting the configuration word.)

Interrupt Status Register(R0F) is the interrupt flag register that recodes the interrupt requests in the relative flags. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Individual interrupts can be enabled/disabled through their corresponding enable bits in Interrupt Mask Register.

When one of the interrupt occurs, the next instruction will be fetched from address 008H.Once in the interrupt service routine, the source of an interrupt can be determined by polling Interrupt Status Register(R0F).The interrupt flag bit must be cleared by program before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts. The RETFIE instruction exits the interrupt routine and enables the global interrupt.

The flag bit (except PBIF bit) in Interrupt Status Register is set by interrupt event regardless of the status of its mask bit or the execution of ENI. Reading the Interrupt Status Register will be the logic AND of the Interrupt Status Register and Interrupt Mask Register.

When an interrupt is generated by the INT instruction, the next instruction will be fetched from address 001h.

3.8.1 External INT Interrupt

External interrupt on INT pin is rising or falling edge triggered can be selected by INTEDG bit of T0MODE Register. When a valid edge appears on the INT pin, then the flag bit EXIF of the Interrupt Status Register is set. Clearing the EXIE bit of Interrupt Mask Register can disable this interrupt.

3.8.2 Timer0 Interrupt

An overflow (FFh → 00h) in the Timer0 register will set the flag bit T0IF. Clearing T0IE bit of the Interrupt Mask Register can disable this interrupt.

3.8.3 Timer1 Interrupt

An underflow (00h → FFh) in the Timer1 register will set the flag bit T1IF. Clearing T1IE bit of the Interrupt Mask Register can disable this interrupt.

3.8.4 Timer2 Interrupt

An underflow (00h → FFh) in the Timer2 register will set the flag bit T2IF. Clearing T2IE bit of the Interrupt Mask Register can disable this interrupt.

3.8.5 Port B Input Change Interrupt

An input change on PB<7:0> will set the flag bit PBIF. Clearing PBIE bit of the Interrupt Mask Register can disable this interrupt.

Setting the PortB Input Change Interrupt Control Register (F9) can enable the PortB Input Change Interrupt individually. Reading PortB is necessary before the port B input change interrupt is enabled. When the pin is configured as output, the Input Change Interrupt function will be disabled.

3.8.6 Watchdog timer out Interrupt

Programming configuration word can enable the watchdog interrupt function. If this function is enabled, a WDT time-out will set the flag bit WDTIF. Clearing WDTIE bit of the Interrupt Mask Register can disable this interrupt.

3.9 Power-Down Mode (Sleep)

Executing a SLEEP instruction enters power-down mode. When SLEEP instruction is executed, the PD bit of Status register will be cleared, the TO bit will be set, the Watchdog Timer will be cleared and keeps running, and the oscillator driver is turned off. All I/O pins maintain the status they had before the SLEEP instruction was executed.

3.9.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events.

1. External reset input on Reset pin.
2. WDT time-out reset or WDT time-out interrupt (depend on which one is enabled by setting configuration word).
3. Interrupt from PD1/INT pin, or PortB change interrupt. (if enabled)

External reset input on Reset pin and WDT time-out reset will cause a device reset. The PD and TO bits can be used to determine the cause of device reset. The PD bit is set on power-up and is cleared when SLEEP instruction is executed. The TO bit is cleared if a WDT reset occurred.

An interrupt event is intended to wake-up the device, the corresponding interrupt function should be enabled before SLEEP. If ENI is executed before SLEEP, the program will branch to the interrupt address (008h) after wake-up. If DISI is executed before SLEEP, the device will continue execution at the instruction next to SLEEP instruction after wake-up.

3.10 Configuration Word

Bit	Name	Function
2,1,0	Fosc<2:0>	=000, EXT-R mode (External resistor and internal capacitor), PA6/Xin/Rin pin will connect to Rext and PA7/Xout pin will output instruction clock. =001, IRC mode (Internal RC), PA6/Xin/Rin pin will be assigned to PA6 and *PA7/Xout pin will output instruction clock*. =011, IRC mode (Internal RC), PA6/Xin/Rin pin will be assigned to PA6 and *PA7/Xout pin will be assigned to PA7*. =100, LF-XTAL mode. =101, XTAL mode. =110, HF-XTAL mode. =111, ERC mode (External RC), PA7/Xout pin will output instruction clock. *(Default)*
5,4,3	IEF<2:0>	IRC / EXT-R frequency selection = 000, IRC= 20MHz = 001, IRC= 16MHz = 010, IRC= 8MHz = 011, IRC= 4MHz = 100, IRC= 2MHz = 101, IRC= 1MHz = 110, IRC = 455KHz = 111, IRC = 32KHz *(Default)*
6	WDTEN	=1, Watchdog Timer enable *(Default)* =0, Watchdog Timer disable
7	WDTREN	=1, Watchdog Timer reset enable *(Default)* =0, Watchdog Timer interrupt enable
8	CLK	Instruction period selection =1, four oscillator periods *(Default)* =0, two oscillator periods
11,10,9	LVR<2:0>	Precise Low voltage reset selection =001, enable, LVR voltage = 2.0V =010, enable, LVR voltage = 2.6V =011, enable, LVR voltage = 2.8V =100, enable, LVR voltage = 3.2V =101, enable, LVR voltage = 3.6V =110, enable, LVR voltage = 4.3V =111, disable *(Default)*
12	PA5EN	Pin Function Selection of PA5/Reset =1, assigned to Reset function and force PA5/Reset to input Pin *(Default)* =0, assigned to PA5 digital I/O function
13	Code-protect	=1, EPROM unprotected *(Default)* =0, EPROM protected

4. Instruction Set

AM8EB057A include total 55 instructions, and summarized in the following table.

Mnemonic Operands	Description	Cycles	Instruction Code	Status Affected
NOP	No operation	1	00 0000 0000 0000	-
SLEEP	Go into standby mode	1	00 0000 0000 0001	TO, PD
CLRWDT	Clear Watchdog Timer	1	00 0000 0000 0010	TO, PD
T0MODE	Load T0MODE Register	1	00 0000 0000 0011	-
ENI	Enable Interrupt	1	00 0000 0000 0100	
IOST F	Load IOST Register	1	00 0000 0000 ffff	-
RET	Return from subroutine	2	00 0000 0001 0000	-
RETIE	Return from interrupt, Enable Interrupt	2	00 0000 0001 0001	-
DAA	Decimal Adjust ACC	1	00 0000 0001 0010	C
DISI	Disable Interrupt	1	00 0000 0001 0011	-
T0MODER	Move T0MODE Register to ACC	1	00 0000 0001 0100	-
IOSTR F	Move IOST Register to ACC	1	00 0000 0001 ffff	-
SFUN S	Load SFUN Register	1	00 0000 0010 ssss	-
SFUNR S	Move SFUN Register to ACC	1	00 0000 0011 ssss	-
MOVAR R	Move ACC to R	1	00 0000 1rrr rrrr	-
MOVR R, d	Move R	1	00 0001 drrr rrrr	Z
CLRA	Clear ACC	1	00 0010 0000 0000	Z
INT	S/W interrupt	3	00 0010 0001 0000	-
TABLEA	Read ROM Code to TBH and ACC	2	00 0010 0001 0001	-
CALLA	Call subroutine	2	00 0010 0001 0010	-
GOTOA	Unconditional branch	2	00 0010 0001 0011	-
CLRR R	Clear R	1	00 0010 1rrr rrrr	Z
ADDAR R, d	Add ACC and R	1	00 0011 drrr rrrr	C, DC, Z
SUBAR R, d	Subtract ACC from R	1	00 0100 drrr rrrr	C, DC, Z
INCR R, d	Increment R	1	00 0101 drrr rrrr	Z
DECR R, d	Decrement R	1	00 0110 drrr rrrr	Z
COMR R, d	Complement R	1	00 0111 drrr rrrr	Z
ANDAR R, d	AND ACC with R	1	00 1000 drrr rrrr	Z
IORAR R, d	Inclusive OR ACC with R	1	00 1001 drrr rrrr	Z
XORAR R, d	Exclusive OR ACC with R	1	00 1010 drrr rrrr	Z
RRR R, d	Rotate right R	1	00 1011 drrr rrrr	C
RLR R, d	Rotate left R	1	00 1100 drrr rrrr	C
SWAPR R, d	Swap halves R	1	00 1101 drrr rrrr	-
INCRSZ R, d	Increment R, Skip if 0	1 or 2(skip)	00 1110 drrr rrrr	-
DECRSZ R, d	Decrement R, Skip if 0	1 or 2(skip)	00 1111 drrr rrrr	-
RETIA I	Return, place immediate in A	2	01 0000 iiii iiii	-
MOVIA I	Move immediate to ACC	1	01 0001 iiii iiii	-
ANDIA I	AND immediate with ACC	1	01 0010 iiii iiii	Z
IORIA I	Inclusive OR immediate with ACC	1	01 0011 iiii iiii	Z
XORIA I	Exclusive OR immediate with ACC	1	01 0100 iiii iiii	Z
ADDIA I	Add ACC and immediate	1	01 0101 iiii iiii	C, DC, Z
ADCIA I	Add ACC and immediate with Carry	1	01 0110 iiii iiii	C, DC, Z
SUBIA I	Subtract ACC from immediate	1	01 0111 iiii iiii	C, DC, Z

Mnemonic Operands	Description	Cycles	Instruction Code	Status Affected
SBCIA I	Subtract ACC and Carry from immediate	1	01 1000 iiii iiii	C, DC, Z
CALL I	Call subroutine	2	01 1001 iiii iiii	-
GOTO I	Unconditional branch	2	01 101i iiii iiii	-
ADCAR R, d	Add ACC and R with Carry	1	01 1100 drrr rrrr	C, DC, Z
SBCAR R, d	Subtract ACC and Carry from R	1	01 1101 drrr rrrr	C, DC, Z
CMPAR R	Compare R with ACC	1	01 1110 1rrr rrrr	C, Z
BCR R, bit	Clear bit in R	1	10 11bb brrr rrrr	-
BSR R, bit	Set bit in R	1	10 10bb brrr rrrr	-
BTRSC R, bit	Test bit in R and skip if clear	1 or 2(skip)	10 01bb brrr rrrr	-
BTRSS R, bit	Test bit in R and skip if set	1 or 2(skip)	10 00bb brrr rrrr	-
LCALL I	Call subroutine	2	11 0iii iiii iiii	-
LGOTO I	Unconditional branch	2	11 1iii iiii iiii	-

Legend:

b : Bit position
WDT : Watchdog Timer
R : Register address
i : Immediate data
ACC : Accumulator
T0MODE : T0MODE register
PD : Power down flag
TO : Time overflow bit
IOST : I/O port control register
Z : Zero flag
C : Carry flag
DC : Digital carry flag
I : (i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0)
R : (r_6 r_5 r_4 r_3 r_2 r_1 r_0)
F : (f_3 f_2 f_1 f_0) $_{5\sim f}$
S : (s_3 s_2 s_1 s_0)

d 0 1 : Destination

If d is “0”, the result is stored in the ACC register.

If d is “1”, the result is stored back in register R.

ADCAR (Add ACC and R with Carry)

Syntax: ADCAR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: ACC + R + C → dest

Status Affected: C, DC, Z

Description: Add the contents of the ACC register and register 'R' with Carry. If 'd' is 0, the result is stored in the ACC register. If 'd' is '1', the result is stored back in register 'R'.

Cycles: 1

ADCIA (Add ACC and Immediate with Carry)

Syntax: ADCIA I

Operands: 0≤ I ≤ 255

Operation: ACC + I + C → ACC

Status Affected: C, DC, Z

Description: Add the contents of the ACC register and the 8-bit immediate 'I' with Carry. The result is placed in the ACC register.

Cycles: 1

ADDAR (Add ACC and R)

Syntax: ADDAR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: ACC + R → dest

Status Affected: C, DC, Z

Description: Add the contents of the ACC register and register 'R'. If 'd' is 0, the result is stored in the ACC register. If 'd' is '1', the result is stored back in register 'R'.

Cycles: 1

ADDIA (Add ACC and Immediate)

Syntax: ADDIA I

Operands: 0≤ I ≤ 255

Operation: ACC + I → ACC

Status Affected: C, DC, Z

Description: Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the ACC register.

Cycles: 1

ANDAR (AND ACC and R)

Syntax: ANDAR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: ACC and R → dest

Status Affected: Z

Description: The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0, the result is stored in the ACC register. If 'd' is '1', the result is stored back in register 'R'.

Cycles: 1

ANDIA (AND Immediate with ACC)

Syntax: ANDIA I

Operands: 0≤ I ≤ 255

Operation: ACC AND I → ACC

Status Affected: Z

Description: The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.

Cycles: 1

BCR (Clear Bit in R)

Syntax: BCR R, b

Operands: 0≤ R≤ 127

0 ≤ b≤7

Operation: 0 → R<b>

Status Affected: None

Description: Clear bit 'b' in register 'R'.

Cycles: 1

<u>BSR</u> (Set Bit in R)

Syntax: BSR R, b

Operands: 0≤ R≤ 127

0 ≤ b≤7

Operation: 1 → R<b>

Status Affected: None

Description: Set bit ‘b’ in register ‘R’.

Cycles: 1

<u>BTRSC</u> (Test Bit in R, Skip if Clear)

Syntax: BTRSC R, b

Operands: 0≤ R≤ 127

0 ≤ b≤7

Operation: Skip if R<b> = 0

Status Affected: None

Description: If bit ‘b’ in register ‘R’ is 0, the next instruction is skipped. If bit ‘b’ is 0, the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction..

Cycles: 1(2)

<u>BTRSS</u> (Test Bit in R, Skip if Set)

Syntax: BTRSS R, b

Operands: 0≤ R≤ 127

0 ≤ b≤7

Operation: Skip if R<b> = 1

Status Affected: None

Description: If bit ‘b’ in register ‘R’ is ‘1’, the next instruction is skipped. If bit ‘b’ is ‘1’, the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.

Cycles: 1(2)

<u>CALL</u> (Call Subroutine)

Syntax: CALL I

Operands: 0≤ I ≤255

Operation: PC +1 → Top of Stack;

Status<6:5> → PC<10:9>

“ 0 “ → PC<8>

I → PC<7:0>

Status Affected: None

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The 8-bit immediate address is loaded into PC bits <7:0>. The Status <6:5> load into PC<10:9>, PC<8> is cleared. CALL is a two-cycle instruction.

Cycles: 2

<u>CALLA</u> (Call Subroutine)

Syntax: CALLA

Operands: None

Operation: PC +1 → Top of Stack;

{[TBHP], [ACC]}→ PC< 10:0 >

Status Affected: None

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The content of TBHP and ACC is loaded into PC bits < 10:0 >. CALLA is a two-cycle instruction.

Cycles: 2

<u>CLRA</u> (Clear ACC)

Syntax: CLRA

Operands: None

Operation: 00h → ACC;

1 → Z

Status Affected: Z

Description: The ACC register is cleared. Zero bit (Z) is set.

Cycles: 1

CLRR (Clear R)

Syntax: CLRR R

Operands: 0≤ R≤ 127

Operation: 00h → R;

1 → Z

Status Affected: Z

Description: The contents of register ‘R’ are cleared and the Z bit is set.

Cycles: 1

CLRWDT (Clear Watchdog Timer)

Syntax: CLRWDT

Operands: None

Operation: 00h → WDT;

00h → WDT prescaler (if assigned);

1 → TO;

1 → PD

Status Affected: TO,PD

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set.

Cycles: 1

COMR (Complement R)

Syntax: COMR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: ~R → dest

Status Affected: Z

Description: The contents of register ‘R’ are complemented. If ‘d’ is 0, the result is stored in the ACC register. If ‘d’ is 1, the result is stored back in register ‘R’.

Cycles: 1

CMPAR (Compare ACC and R)

Syntax: CMPAR R

Operands: 0≤ R≤ 127

Operation: R - ACC

Status Affected: C, Z

Description: Compare ACC and R. Subtract (2’s complement method) the ACC register from register ‘R’ that will not change the content of ACC and R.

Cycles: 1

DAA (Adjust ACC’s data format from HEX to DEC)

Syntax: DAA

Operands: None

Operation: If [ACC<3:0> > 9] or [DC=1] then A<3:0> + 6

→ ACC<3:0> ;

If [ACC<7:4 > > 9] or [C=1] then A<7:4> + 6

→ ACC<7:4>

Status Affected: C

Description: Convert the ACC data from hexadecimal to decimal format after addition operation and restored to ACC. DAA instruction must be placed at the next Instruction of addition operation.

Cycles: 1

DECR (Decrement R)

Syntax: DECR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R - 1 → dest

Status Affected: Z

Description: Decrement register ‘R’. If ‘d’ is 0, the result is stored in the ACC register. If ‘d’ is 1, the result is stored back in register ‘R’.

Cycles: 1

DECRSZ (Decrement R, Skip if 0)

Syntax: DECRSZ R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R - 1 → dest; skip if result =0

Status Affected: None

Description: The contents of register ‘R’ are decremented. If ‘d’ is 0, the result is placed in the ACC register. If ‘d’ is 1, the result is placed back in register ’R’. If the result is 0, the next instruction which is already fetched is discarded and a NOP is executed instead making it a two-cycle instruction.

Cycles: 1(2)

DISI (Disable Interrupt)

Syntax: DISI

Operands: None

Operation: 0 → INT;

Status Affected: None

Description: Disable global interrupt.

Cycles: 1

ENI (Enable Interrupt)

Syntax: ENI

Operands: None

Operation: 1 → INT;

Status Affected: None

Description: Enable global interrupt.

Cycles: 1

GOTO (Unconditional Branch)

Syntax: GOTO I

Operands: 0≤ I ≤511

Operation: Status<6:5> → PC<10:9>

I → PC<8:0>

Status Affected: None

Description: GOTO is an unconditional branch. The 9-bit immediate address is loaded into PC bits <8:0>. PC<10:9> is loaded from the Status <6:5>. GOTO is a two-cycle instruction.

Cycles: 2

GOTOA (Unconditional Branch)

Syntax: GOTOA

Operands: None

Operation: {[TBHP], [ACC]}→ PC< 10:0 >

Status Affected: None

Description: GOTOA is an unconditional branch. The content of TBHP and ACC is loaded into PC bits < 10:0 >. GOTOA is a two-cycle instruction.

Cycles: 2

INCR (Increment R)

Syntax: INCR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R + 1 → dest

Status Affected: Z

Description: The contents of register ‘R’ are incremented. If ‘d’ is 0, the result is placed in the ACC register. If ‘d’ is 1, the result is placed back in register ‘R’.

Cycles: 1

INCRSZ (Increment R, Skip if 0)

Syntax: INCRSZ R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R + 1 → dest, skip if result = 0

Status Affected: None

Description: The contents of register ‘R’ are incremented. If ‘d’ is 0, the result is placed in the ACC register. If ‘d’ is 1, the result is placed back in register ‘R’. If the result is 0, the next instruction which is already fetched is discarded and a NOP is executed instead making it a two-cycle instruction.

Cycles: 1(2)

INT (S/W Interrupt)

Syntax: INT

Operands: None

Operation: PC + 1 → Top of Stack,

001h → PC

Status Affected: None

Description: Interrupt subroutine call. First, return address (PC+1) is pushed onto the stack. The address 001h is loaded into PC bits <10:0>.

Cycles: 3

IORAR (OR ACC with R)

Syntax: IORAR R, d

Operands: $0 \leq R \leq 127$

$d \in [0,1]$

Operation: ACC or R → dest

Status Affected: Z

Description: Inclusive OR the ACC register with register ‘R’. If ‘d’ is 0 the result is placed in the ACC register. If ‘d’ is 1 the result is placed back in register ‘R’.

Cycles: 1

IORIA (OR Immediate with ACC)

Syntax: IORIA I

Operands: $0 \leq I \leq 255$

Operation: ACC or I → ACC

Status Affected: Z

Description: The contents of the ACC register are OR’ed with the 8-bit immediate ‘I’. The result is placed in the ACC register.

Cycles: 1

IOST (Load IOST Register)

Syntax: IOST F

Operands: F = 5,6, 7…f

Operation: ACC → IOST register F

Status Affected: None

Description: IOST register ‘F’ (F= 5,6,7…f) is loaded with the contents of the ACC register.

Cycles: 1

IOSTR (Move IOST Register to ACC)

Syntax: IOSTR F

Operands: F = 5,6, 7…f

Operation: IOST register F →ACC

Status Affected: None

Description: Move the contents of IOST register ‘F’ (F= 5,6,7…f) to ACC register.

Cycles: 1

LCALL (Call Subroutine)

Syntax: LCALL I

Operands: $0 \leq I \leq 2047$

Operation: PC +1 → Top of Stack;

I → PC<10:0>

Status Affected: None

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. LCALL is a two-cycle instruction.

Cycles: 2

LGOTO (Unconditional Branch)

Syntax: LGOTO I

Operands: $0 \leq I \leq 2047$

Operation: I → PC<10:0>

Status Affected: None

Description: LGOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. LGOTO is a two-cycle instruction.

Cycles: 2

MOVAR (Move ACC to R)

Syntax: MOVAR R

Operands: 0≤ R≤ 127

Operation: ACC → R

Status Affected: None

Description: Move data from the ACC register to register ‘R’.

Cycles: 1

MOVIA (Move Immediate to ACC)

Syntax: MOVIA I

Operands: 0≤ I ≤ 255

Operation: I → ACC

Status Affected: None

Description: The 8-bit immediate ‘I’ is loaded into the ACC register. The don’t cares will assemble as 0s.

Cycles: 1

MOVR (Move R)

Syntax: MOVR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R → dest

Status Affected: Z

Description: The contents of register ‘R’ is moved to destination ‘d’. If ‘d’ is 0, destination is the ACC register. If ‘d’ is 1, the destination is file register ‘R’. ‘d’ is 1 is useful to test a file register since status flag Z is affected.

Cycles: 1

NOP (No Operation)

Syntax: NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Cycles: 1

RETIE (Return from Interrupt, Enable Interrupt)

Syntax: RETIE

Operands: None

Operation: Top of Stack → PC

Status Affected: None

Description: The program counter is loaded from the top of the stack (the return address) and enable Interrupt function. This is a two-cycle instruction.

Cycles: 2

RETIA (Return with Immediate in ACC)

Syntax: RETIA I

Operands: 0≤ I ≤ 255

Operation: I → ACC;

Top of Stack → PC

Status Affected: None

Description: The ACC register is loaded with the 8-bit immediate ‘I’. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Cycles: 2

RET (Return from Subroutine)

Syntax: RET

Operands: None

Operation: Top of Stack → PC

Status Affected: None

Description: The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Cycles: 2

<u>RLR</u> (Rotate Left f through Carry)

Syntax: RLR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R<7> → C;

R<6:0> → dest<7:1>;

C → dest<0>

Status Affected: C

Description: The contents of register 'R' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the ACC register. If 'd' is 1, the result is stored back in register 'R'.

Cycles: 1

<u>RRR</u> (Rotate Right f through Carry)

Syntax: RRR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: C → dest<7>;

R<7:1> → dest<6:0>;

R<0> → C

Status Affected: C

Description: The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the ACC register. If 'd' is 1, the result is placed back in register 'R'.

Cycles: 1

<u>SBCAR</u> (Subtract ACC and Carry from R)

Syntax: SUBAR R, d

Operands: 0≤ R≤ 127

d∈[0,1]

Operation: R - ACC - C → dest

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the ACC and Carry register from register 'R'. If 'd' is 0, the result is stored in the ACC register. If 'd' is 1, the result is stored back in register 'R'.

Cycles: 1

<u>SBCIA</u> (Subtract ACC and Carry from Immediate)

Syntax: SBCIA I

Operands: 0≤ I ≤ 255

Operation: I - ACC - C→ ACC

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the ACC register and Carry from the 8-bit immediate 'I'. The result is placed in the ACC register.

Cycles: 1

<u>SFUN</u> (Load SFUN Register)

Syntax: SFUN S

Operands: S = 0,1,2…

Operation: ACC → SFUN register S

Status Affected: None

Description: SFUN register 'S' (S=0,1,2…) is loaded with the contents of the ACC register.

Cycles: 1

<u>SFUNR</u> (Move SFUN Register to ACC)

Syntax: SFUNR S

Operands: S = 0,1,2…

Operation: SFUN register S →ACC

Status Affected: None

Description: Move the contents of SFUN register 'S' (S= 0,1,2…) to ACC register.

Cycles: 1

SLEEP (Enter SLEEP Mode)

Syntax: SLEEP

Operands: None

Operation: 00h → WDT;

00h → WDT prescaler;

1 → TO;

0 → PD

Status Affected: TO,PD

Description: Time-out status bit (TO) is set. The power-down status bit (PD) is cleared. The WDT and its prescaler are cleared. The processor is put into SLEEP mode.

Cycles: 1

SUBAR (Subtract ACC from R)

Syntax: SUBAR R, d

Operands: $0 \leq R \leq 127$

$d \in [0,1]$

Operation: R - ACC → dest

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0, the result is stored in the ACC register. If 'd' is 1, the result is stored back in register 'R'.

Cycles: 1

SUBIA (Subtract ACC from Immediate)

Syntax: SUBIA I

Operands: $0 \leq I \leq 255$

Operation: I - ACC → ACC

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is placed in the ACC register.

Cycles: 1

SWAPR (Swap nibbles in R)

Syntax: SWAPR R, d

Operands: $0 \leq R \leq 127$

$d \in [0,1]$

Operation: R<3:0> → dest<7:4>;

R<7:4> → dest<3:0>

Status Affected: None

Description: The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0, the result is placed in ACC register. If 'd' is 1, the result in placed in register 'R'.

Cycles: 1

TABLEA (Read ROM Code to TBH and ACC)

Syntax: TABLEA

Operands: None

Operation: ROM code { [TBHP],[ACC] }<7:0> → ACC

ROM code { [TBHP],[ACC] }<13:8> → TBH

Status Affected: None

Description: Move the low byte of the addressed ROM code to ACC and move the high byte of the addressed ROM code to TBH.

Cycles: 2

T0MODE (Load T0MODE Register)

Syntax: T0MODE

Operands: None

Operation: ACC → T0MODE

Status Affected: None

Description: The content of the ACC register is loaded into the T0MODE register.

Cycles: 1

<u>T0MODER</u> (Move T0MODE Register to ACC)

Syntax: T0MODER

Operands: None

Operation: T0MODE → ACC

Status Affected: None

Description: Move the content of T0MODE register to ACC register.

Cycles: 1

<u>XORAR</u> (Exclusive OR ACC with R)

Syntax: XORAR R, d

Operands: $0 \leq R \leq 127$

$d \in [0,1]$

Operation: ACC xor R → dest

Status Affected: Z

Description: Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0, the result is stored in the ACC register. If 'd' is 1, the result is stored back in register 'R'.

Cycles: 1

<u>XORIA</u> (Exclusive OR Immediate with ACC)

Syntax: XORIA I

Operands: $0 \leq I \leq 255$

Operation: ACC xor I → ACC

Status Affected: Z

Description: The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.

Cycles: 1

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD}~V_{SS}	-0.5 ~ +6.0	V
V_{in}	V_{SS}-0.3 < V_{in} < V_{DD}+0.3	V
V_{out}	GND < V_{out} < V_{DD}	V
T_{op} (operating)	-40 ~ +85	ºC
T_{st} (storage)	-65 ~ +150	ºC

5.2 DC Characteristics (Top = 25ºC)

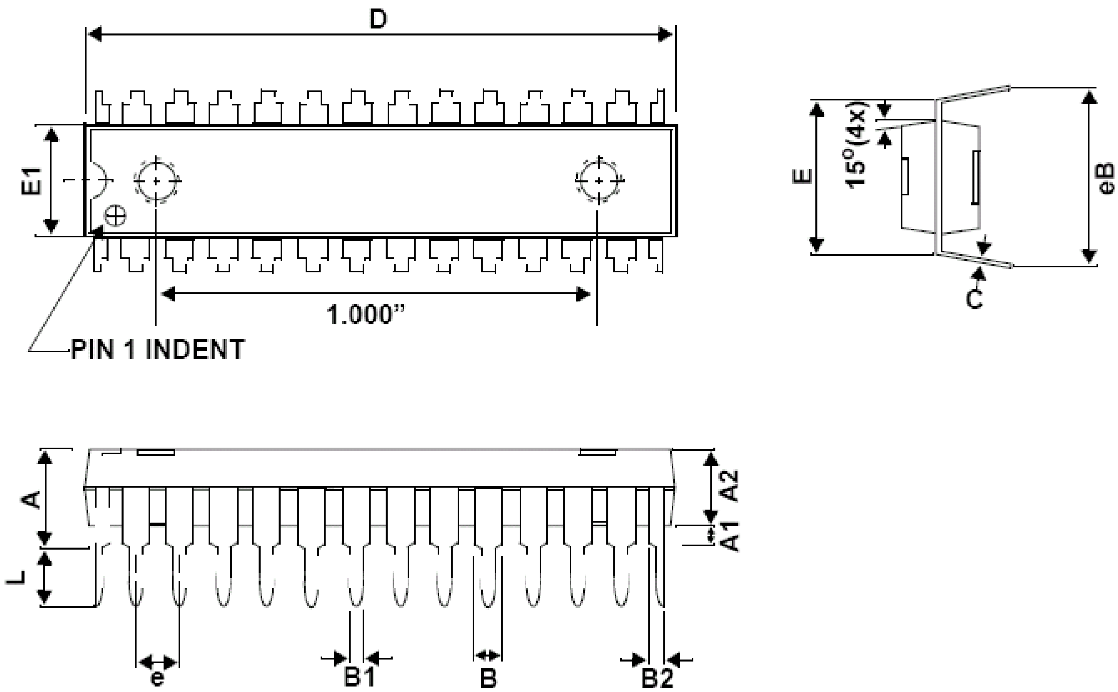
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{DD1}	Operating voltage range	20MHz at HF-XTAL	2.6	3	5.5	V
V_{DD2}		4MHz at XTAL	2.2	3	5.5	
V_{DD3}		32kHz at LF-XTAL	2.0	3	5.5	
F_{HF}	HF-XTAL mode freq., V_{DD}=5V	Four oscillator periods			20	MHz
	HF-XTAL mode freq., V_{DD}=3V				20	
F_{XT}	XTAL mode freq., V_{DD}=5V	Four oscillator periods			10	MHz
	XTAL mode freq., V_{DD}=3V				10	
F_{LF}	LF-XTAL mode freq., V_{DD}=5V	Four oscillator periods			400	KHz
	LF-XTAL mode freq., V_{DD}=3V				400	
F_{ERC}	ERC mode freq., V_{DD}=5V	Rext=1Kohm; Cext=3.3pF			12	MHz
	ERC mode freq., V_{DD}=3V				8	
V_{ih}	Input high voltage, V_{DD}=5V	I/O port	2.0			V
		RTCC	4.0			
		RESET	3.3			
	Input high voltage, V_{DD}=3V	I/O port	1.5			
		RTCC	2.4			
		RESET	2			
V_{il}	Input low voltage, V_{DD}=5V	I/O port			1.0	V
		RTCC			1.0	
		RESET			0.4	
	Input low voltage, V_{DD}=3V	I/O port			0.5	
		RTCC			0.5	
		RESET			0.3	
V_{oh}	Output high voltage, V_{DD}=5V	I_{oh} = -14mA	4.0			V
	Output high voltage, V_{DD}=3V		1.6			
V_{ol}	Output low voltage, V_{DD}=5V	I_{ol} = 14mA			0.4	V
	Output low voltage, V_{DD}=3V				0.5	
I_{oh}	I/O Port Output high current, V_{DD}=5V	V_{oh} = 4.0 V		-19.4		mA
	I/O Port Output high current, V_{DD}=3V	V_{oh} = 2.0 V		-12.2		
I_{ol}	I/O Port Output low current, V_{DD}=5V	V_{ol} = 1.0V		72		
	I/O Port Output low current, V_{DD}=3V	V_{ol} = 1.0V		46		

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Icol	PB1/IR constant output low current, VDD=5V	Vol=1.0V		48		mA
	PB1/IR constant output low current, VDD=3V	Vol=1.0V		45		
	PB1/IR constant output low current, VDD=2.4V	Vol=1.0V		44		
Iil	Internal Pull-high current, VDD=5V	Input pin at VSS		-58		uA
	Internal Pull-high current, VDD=3V			-19		
Iih	Internal Pull-low current, VDD=5V	Input pin at VDD		38		uA
	Internal Pull-low current, VDD=3V			12		
Isb	Power-down current, VDD=5V	Sleep mode, WDT enable		8		uA
		Sleep mode, WDT disable		1		
	Power-down current, VDD=3V	Sleep mode, WDT enable		1.9		
		Sleep mode, WDT disable		1		
Iop1	HF-XTAL, VDD=5V, 4 clock Instruction (WDT enable)	20MHz		4.9		mA
		16MHz		4.0		
		10MHz		2.7		
	HF-XTAL, VDD=3V, 4 clock Instruction (WDT enable)	20MHz		2.8		mA
		16MHz		2.3		
		10MHz		1.5		
	XTAL, VDD=5V, 4 clock Instruction (WDT enable)	8MHz		2.1		mA
		4MHz		1.2		
		1MHz		702		uA
		455KHz		461		
	XTAL, VDD=3V, 4 clock Instruction (WDT enable)	8MHz		1.2		mA
		4MHz		627		uA
		1MHz		205		
		455KHz		155		
	LF-XTAL, VDD=5V, 4 clock Instruction (WDT enable)	32.768KHz		25		uA
	LF-XTAL, VDD=3V, 4 clock Instruction (WDT disable)	32.768KHz		10		
Iop2	IRC mode VDD=5V, 4 clock Instruction (WDT enable)	20MHz		6.4		mA
		16MHz		5.2		
		8MHz		2.8		
		4MHz		1.7		
		2MHz		1.0		
		1MHz		635		uA
		455KHz		412		
		32.768KHz		51		
	IRC mode, VDD=3V, 4 clock Instruction (WDT enable)	20MHz		3.7		mA
		16MHz		3.1		
		8MHz		1.7		
		4MHz		1.0		
		2MHz		570		uA

Symbol	Description	Condition			Min.	Typ.	Max.	Unit
		1MHz				339		
		455KHz				206		
		32.768KHz				25		
I_{op3}	ERC mode, V_{DD}=5V, 4 clock Instruction (WDT enable)	***Cext***	***Rext***	***OSC Freq.***				
		3.3p	1K	F=12.8MHz		7.5		mA
			3.3K	F=7.4MHz		3.6		
			5.1K	F=5.5MHz		2.6		
			10K	F=3.2MHz		1.5		
			100K	F=396KHz		186		uA
		20p	1K	F=10 MHz		6.5		mA
			3.3K	F=4.9MHz		2.7		
			5.1K	F=3.4MHz		1.9		
			10K	F=1.9MHz		1.0		
			100K	F=221KHz		127		UA
		100p	1K	F=4.8MHz		4.6		mA
			3.3K	F=1.9MHz		1.5		
			5.1K	F=1.3MHz		1.0		
			10K	F=669KHz		547		uA
			100K	F=72KHz		72		
		300p	1K	F=2.3MHz		3.5		mA
			3.3K	F=845KHz		1.2		
			5.1K	F=562KHz		764		uA
			10K	F=289KHz		397		
			100K	F=30KHz		59		
	ERC mode, V_{DD}=3V, 4 clock Instruction (WDT enable)	3.3p	1K	F=8.2MHz		3.5		mA
			3.3K	F=6.0MHz		1.9		
			5.1K	F=4.8MHz		1.4		
			10K	F=3.1MHz		867		uA
			100K	F=445KHz		119		
		20p	1K	F=6.9MHz		3.3		mA
			3.3K	F=4.4MHz		1.5		
			5.1K	F=3.4MHz		1.1		
			10K	F=2.0MHz		625		uA
			100K	F=254KHz		79		
		100p	1K	F=4.2MHz		2.7		mA
			3.3K	F=1.9MHz		966		uA
			5.1K	F=1.4MHz		661		
			10K	F=742KHz		354		
			100K	F=83KHz		43		
		300p	1K	F=2.3MHz		2.2		mA
			3.3K	F=926KHz		753		uA
			5.1K	F=628KHz		496		
			10K	F=330KHz		259		
			100K	F=35KHz		35		

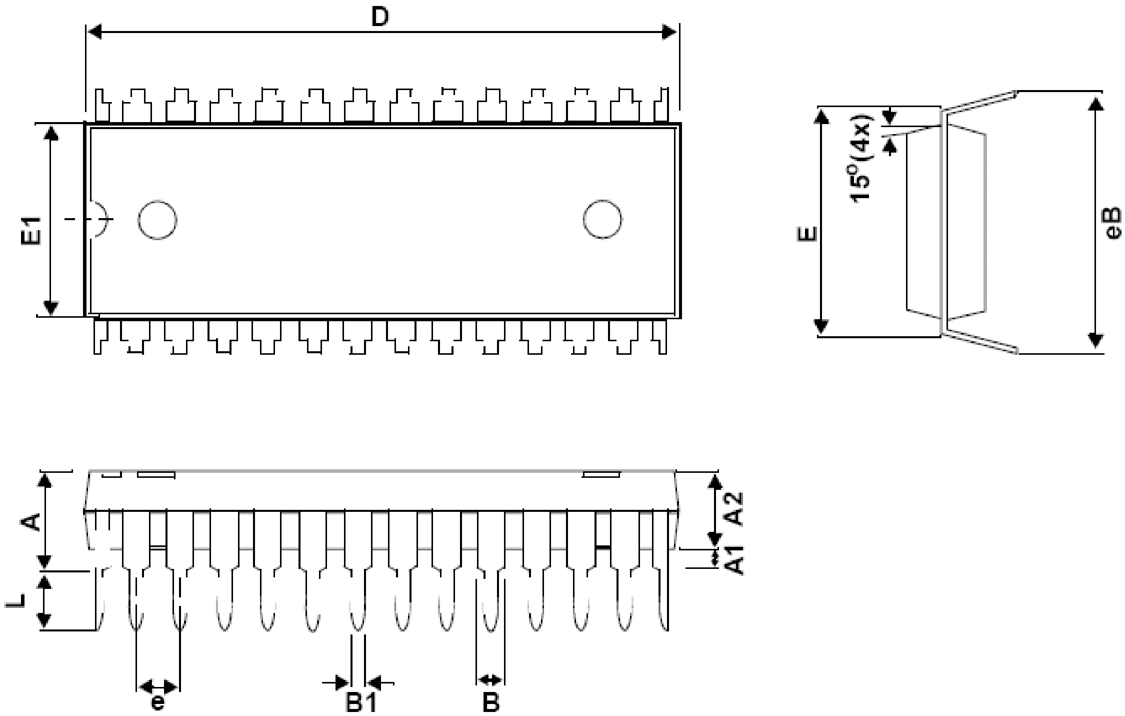
6. Package Dimension

6.1 28 Pin Skinny DIP 300 mil



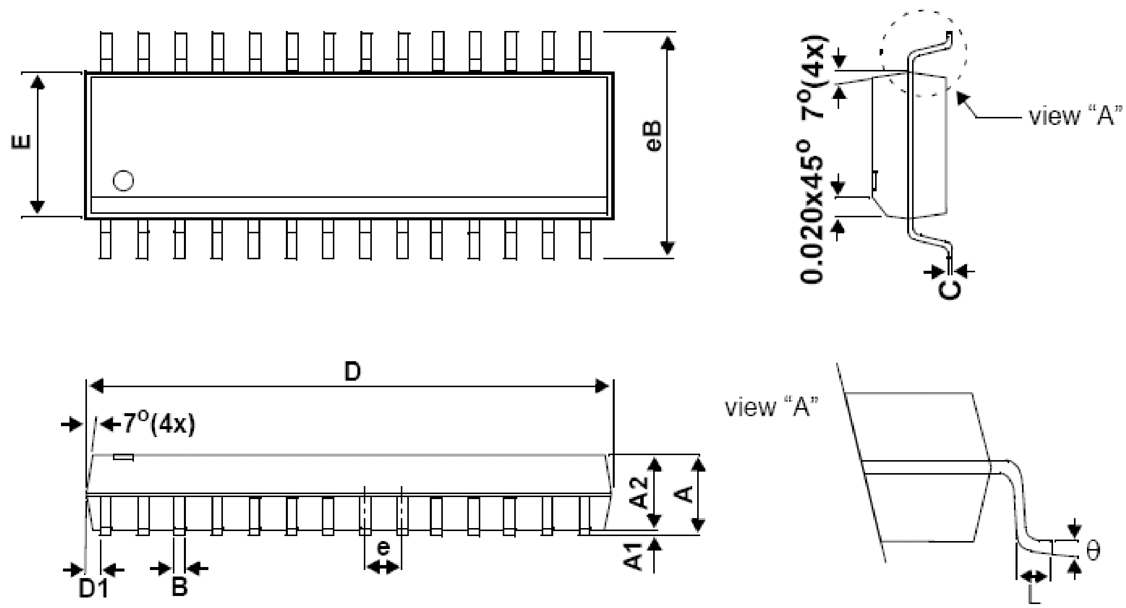
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	4.57	-	-	0.180
A1	0.38	-	-	0.015	-	-
A2	-	3.30	3.56	-	0.130	0.140
B	1.02	-	1.65	0.0040	-	0.065
B1	0.41	-	0.58	0.016	-	0.023
B2	0.71	-	1.12	0.028	-	0.044
C	0.20	0.25	0.33	0.008	0.010	0.013
D	35.13	35.18	35.43	1.383	1.385	1.395
E	7.87	8.31	8.38	0.310	0.327	0.330
E1	7.26	7.32	7.52	0.284	0.288	0.296
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
eB	8.64	-	9.65	0.340	-	0.380

6.2 28 Pin DIP 600 mil



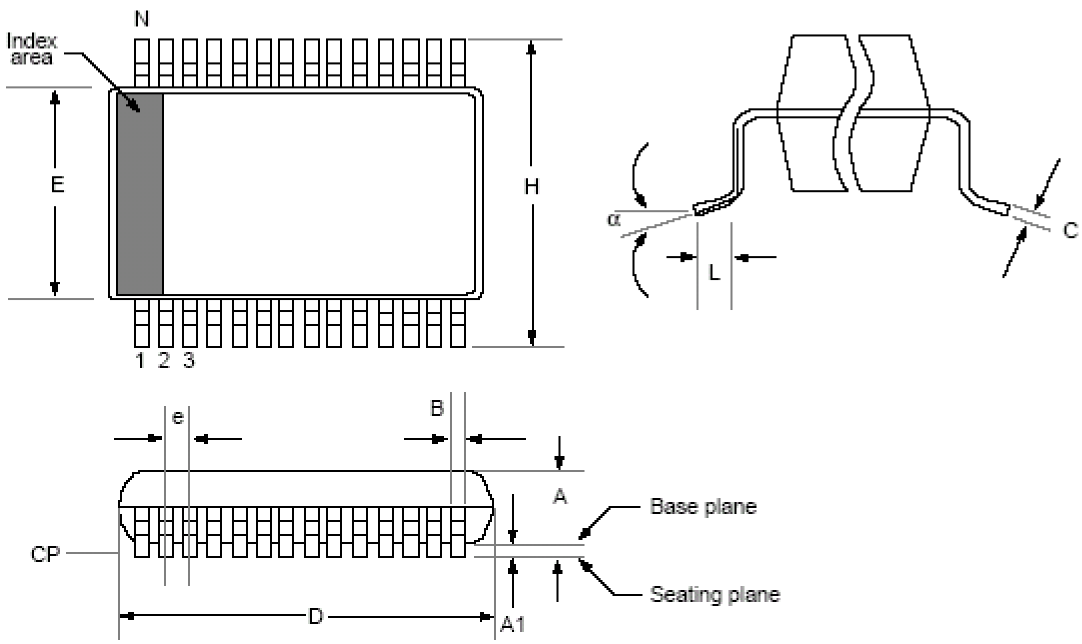
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	5.59	-	-	0.220
A1	0.38	-	-	0.015	-	-
A2	3.81	3.94	4.06	0.150	0.155	0.160
B	-	1.52	-	-	0.06	-
B1	-	0.46	-	-	0.018	-
D	36.96	37.08	37.34	1.455	1.460	1.470
E	-	15.24	-	-	0.600	-
E1	13.72	13.84	13.97	0.540	0.545	0.550
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-
eB	16.00	16.51	17.02	0.630	0.650	0.670

6.3 28 Pin SOP 300 mil



Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	2.488	2.743	-	0.098	0.108
A1	0.152	-	-	0.006	-	-
A2	2.21	2.336	2.464	0.087	0.091	0.097
B	0.305	0.406	0.508	0.012	0.016	0.020
C	0.204	0.254	0.304	0.008	0.010	0.012
D	17.78	17.91	18.42	0.700	0.705	0.725
E	7.366	7.493	7.62	0.290	0.295	0.300
e	1.219	1.270	1.321	0.048	0.050	0.052
eB	10.26	10.42	10.57	0.404	0.410	0.416
L	0.635	-	-	0.025	-	-
θ	0°	4°	8°	0°	4°	8°
D1	0.356	0.508	-	0.014	0.020	-

6.4 28 Pin SSOP 209 mil



Package Group: Plastic SSOP						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	1.730	1.990		0.068	0.078	
A1	0.050	0.210		0.002	0.008	
B	0.250	0.380		0.010	0.015	
C	0.130	0.220		0.005	0.009	
D	10.070	10.330		0.396	0.407	
E	5.200	5.380		0.205	0.212	
e	0.650	0.650	Reference	0.026	0.026	Reference
H	7.650	7.900		0.301	0.311	
L	0.550	0.950		0.022	0.037	
N	28	28		28	28	
CP	-	0.102		-	0.004	

7. Ordering Information

P/N	Package Type	Pin Count	Package Size
AM8EB057A	Die	28	-
AM8EB057AP	Skinny DIP	28	300 mil
AM8EB057AW	DIP	28	600 mil
AM8EB057AS	SOP	28	300 mil
AM8EB057AD	SSOP	28	209 mil