1. Feature

ROM: 1K x 14 bits

RAM: 49 x 8 bits / 25 x 8bits

STACK: 4 Levels

I/O ports: 12 / 16 I/O PAD

(a) 8 Pull High I/O PAD from Port B (PULL-Hi resister=54K(Vdd=5V))

(b) 4 normal I/O PAD from Port A

(c) 4 special I/O PAD from EXT_CLK, RESETB1 (Input only), OSC2 and OSC1
(Only In Advance mode, assign to PA4 ~ PA7)

Timer/counter: 8 bits x 3 (TMR0, TMR1, TMR2)
TMR1 and TMR2 can connect be a 16 bits x 1 timer

Prescaler: 3Bits

Five IRQ sources: 3 Internal IRQ, when TMR0, TMR1, TMR2 count overflow
2 External IRQ: PA0/RESETB0/INT0, PA5/RESETB1/INT1

Watchdog Timer: On chip WDT is based on an internal RC oscillator (for WDT used only).
Has 4 mode period can be selected: 1mS, 4mS, 8mS, and 16mS.
User can extend the WDT overflow period by using prescaler.

Reset mode: (a) Power-On reset
(b) Low voltage reset
(c) 2 External Pin reset (PA0/RESETB0/INT0, PA5/RESETB1/INT1)
(d) Watchdog timer count overflow reset

Reset Timer: 16mS (5V)

Four external Oscillate modes: RC, LP Crystal, NT Crystal and HS Crystal.

One internal RC oscillator: 4M Hz (for user used)

Two operation modes: General mode and Advanced mode

Operation Voltage: 2.2V 5.5V
Instruction set: 79

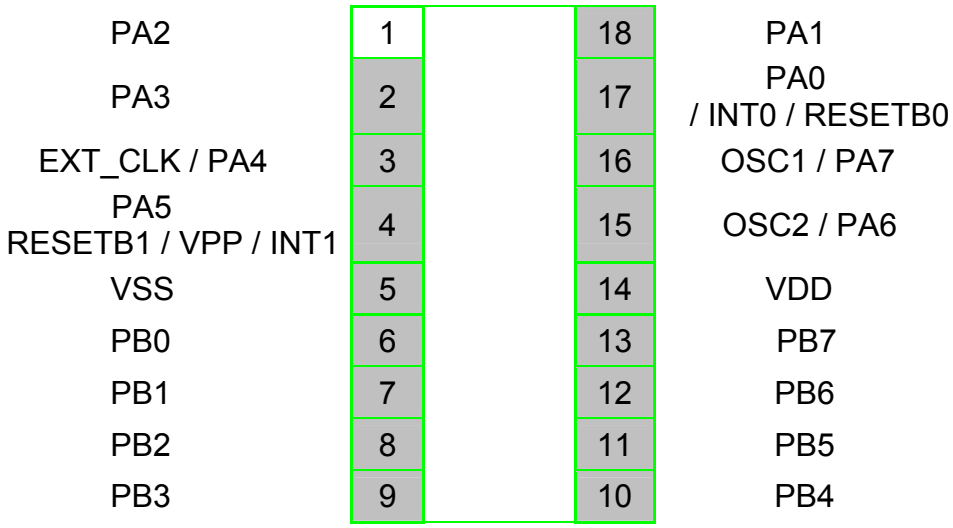
Wake-up mode: Port B (PB7~PB0) Pin Change wakeup
Wake up time can be set by WDTSEL register (23H)

Reset vector: 3FFH
IRQ vector: 3FEH

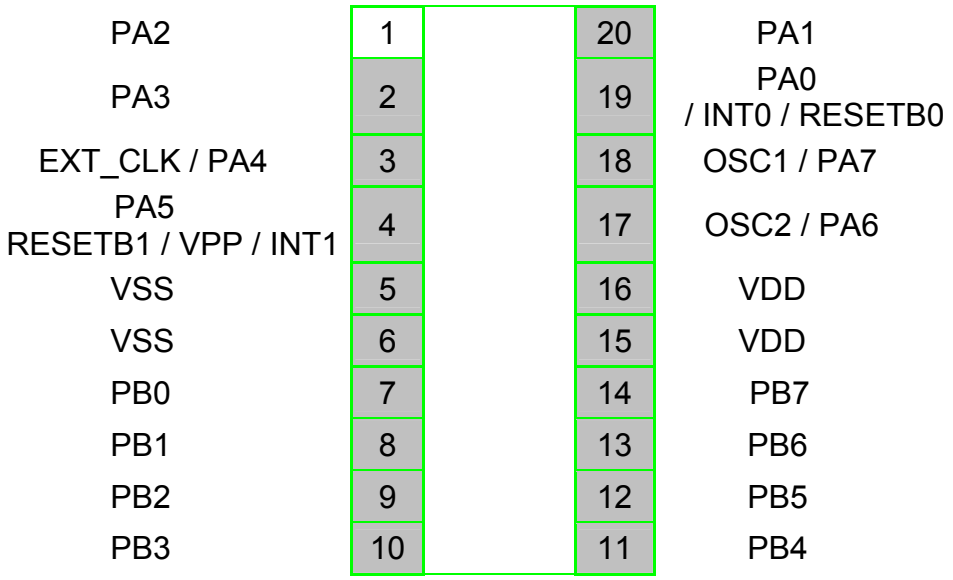
Package Type: TM58PE10SS20C
TM58PE10D18C
TM58PE10S18C
TM58PE10D14C
TM58PE10S14C

2. Pin Definition & Pad Assignment

2.1 18 Pin & 20 Pin

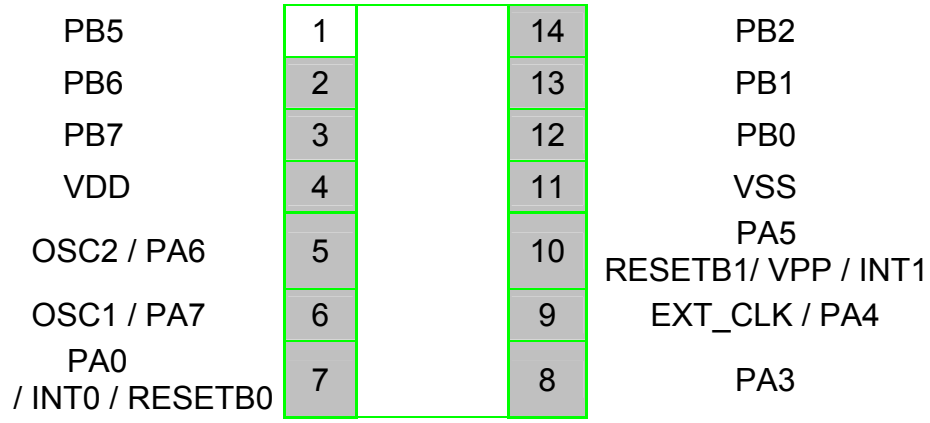


18 Pin Package Types : DIP (TM58PE10D18C)
SOP (TM58PE10S18C)

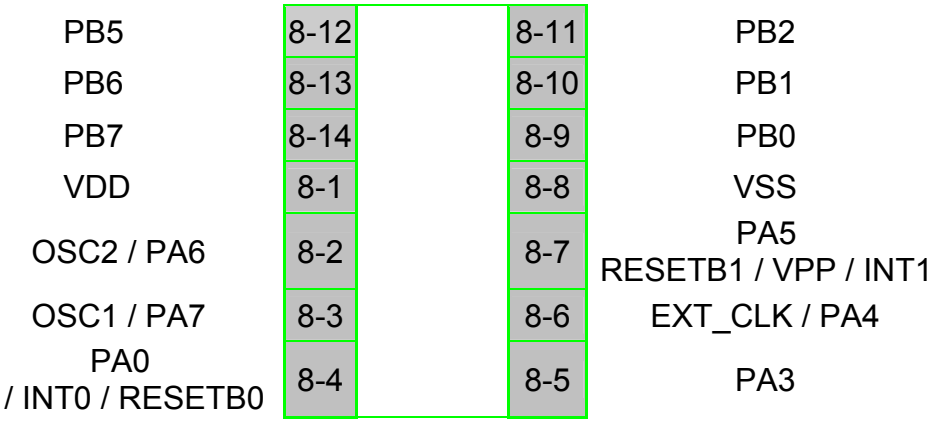


20Pin Package Type: SSOP (TM58PE10SS20C)

2.2 14 Pin



14 Pin Package Type: DIP (TM58PE10D14C)
SOP(TM58PE10S14C)



COB Type

3. PIN Description

3.1 18 Pin

Pin name	Pin No.	Type	Description
PA2 PA3	1 2	I/O	1. I/O pin
EXT_CLK / PA4	3	I/O	1. External clock input to TMR0, TMR1, TMR2 counter 2. I/O pin
PA5 RESETB1/ VPP / INT1	4	Input Only	1. System Reset Pin, triggered by falling edge (Set in configuration word) 2. External interrupt Pin, triggered by falling edge 3. High voltage input Pin 4. Input pin
VSS	5	P	Ground input
PB0 ~ PB7	6 ~ 13	I/O	1. In Advance mode, wakeup from sleep mode when pin change 2. I/O pin (pull-high option)
VDD	14	P	Power input
PA6 / OSC2	15	I/O, O	1. Oscillator output pin 2. I/O pin (set in configuration word)
PA7 / OSC1	16	I/O, I	1. Oscillator input pin 2. I/O pin (set in configuration word)
PA0 / RESETB0/ INT0	17	I/O	1. System Reset pin, triggered by falling edge (Set in configuration word) 2. External interrupt pin, triggered by falling edge 3. I/O pin
PA1	18	I/O	1. I/O pin

3.2 14 Pin

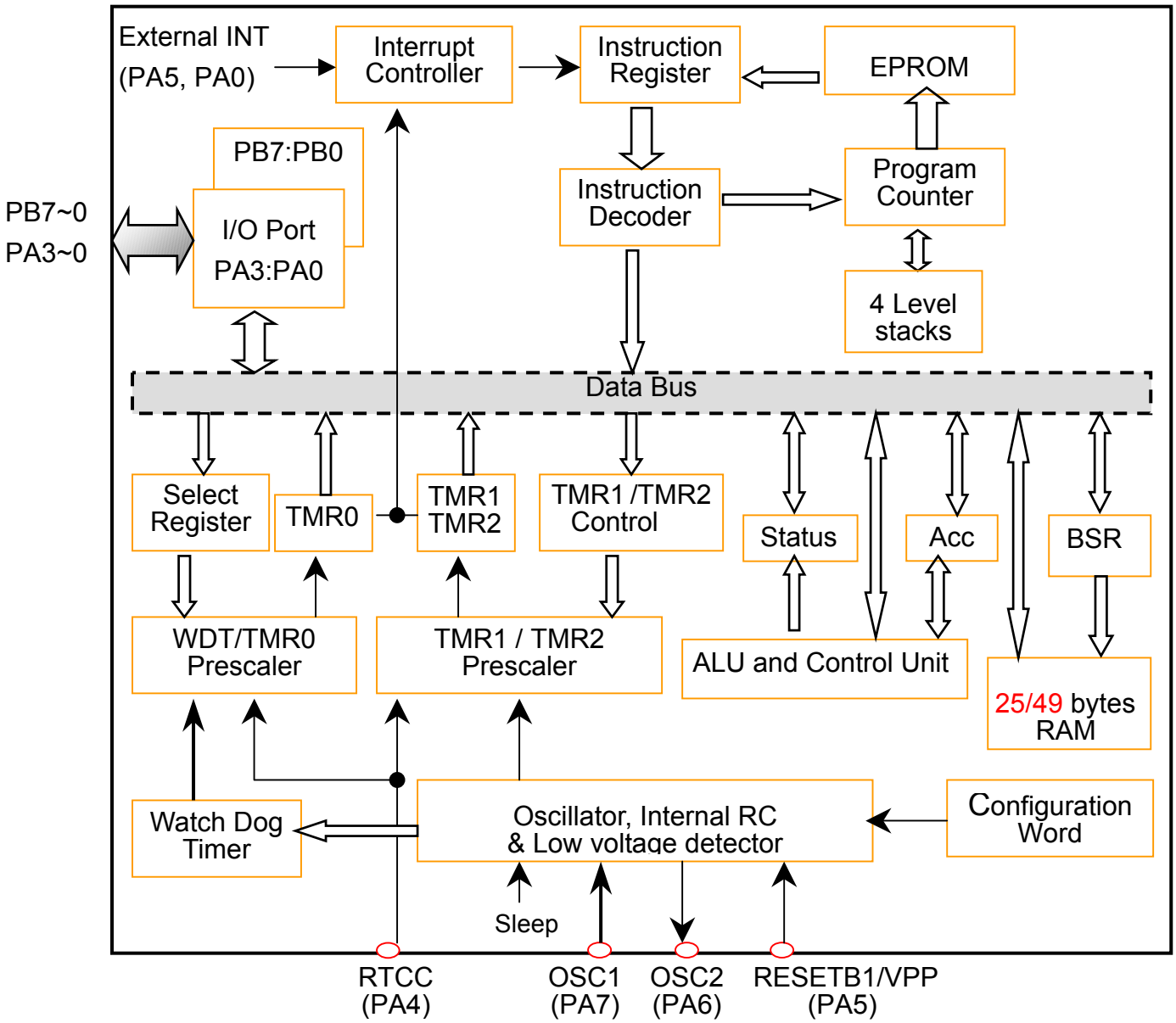
Pin name	Pin No.	Type	Description
PB5 ~ PB7	1~ 3	I/O	1. In Advance mode, wakeup from sleep mode when pin change 2. I/O pin (pull-high option)
VDD	4	P	Power input
PA6 / OSC2	5	I/O, O	1. Oscillator output pin 2. I/O pin (set in configuration word)
PA7 / OSC1	6	I/O, I	1. Oscillator input pin 2. I/O pin (set in configuration word)
PA0 /RESETB0/ INT0	7	I/O	1. System Reset pin, triggered by falling edge (Set in configuration word) 2. External interrupt pin, triggered by falling edge 3. I/O pin
PA3	8	I/O	1. I/O pin
EXT_CLK / PA4	9	I/O	1. External clock input to TMR0 ,TMR1, TMR2 counter 2. I/O pin
PA5 RESETB1/ VPP/ INT1	10	Input Only	1. System Reset Pin, triggered by falling edge (Set in configuration word) 2. External interrupt pin, triggered by falling edge 3. High voltage input pin 4. Input pin
VSS	11	P	Ground input
PB0 ~ PB2	12~ 14	I/O	1. In Advance mode, wakeup from sleep mode when pin change 2. I/O pin (pull-high option)

4.Control Register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SELECT				SUR0	EDGE0	PSA	PS2	PS1	PS0
IAR	$00		A6	A5	A4	A3	A2	A1	A0
TMR0	$01	D7	D6	D5	D4	D3	D2	D1	D0
PC	$02	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	$03		A8	SA0 (A9)	$\overline{TO}$	$\overline{PD}$	Z	DC	C
BSR	$04		D6	D_5	D4	D3	D2	D1	D0
I/O PortA	$05	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
I/O PortB	$06	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PULL-Hi	$20	PUH7	PUH6	PUH5	PUH4	PUH3	PUH2	PUH1	PUH0
IRQM	$21	INTM		TMR2M	TMR1M		EXINTM1	EXINTM0	TMR0M
IRQF	$22			TMR2F	TMR1F		EXINTF1	EXINTF0	TMR0F
WDTSEL	$23							S1	S0
TMR1 Control	$24	TMR1EN	Load	SUR1	SUR0	EDGE	PS2	PS1	PS0
TMR2 Control	$25	TMR2EN	Load	SUR1	SUR0	EDGE	PS2	PS1	PS0
TMR1 Preload	$26	D7	D6	D5	D4	D3	D2	D1	D0
TMR2 preload	$27	D7	D6	D5	D4	D3	D2	D1	D0
WAKE_UP	$40	WDTS	WUE	RTCEN				EIS1	EIS0

Select range function only in Advanced mode.

5. System Block Diagram



6. Memory Map

TM58PE10 memory is organized into program memory and data memory.

6.1 Program memory

TM58PE10 provides 2 program memory map modes, general mode and advanced mode. User can select different mode by setting configuration word.

In general mode, there are only 512 words of the same page that can be directly addressed. Extra program memory can be addressed by setting bit 5 of status register. The sequence of instructions is controlled via the program counter (PC), which automatically increases 1. However, the sequence can be changed by skip, call, goto, lcall and lgoto instructions or by moving data to the PC.

In advanced mode, TM58PE10 allow directly address any address in 1K memories without limited by page size. In addition, lcall and lgoto instructions are employed to provide flexible addressing mode.

TM58PE10 has a 10-bits program counter capable of accessing 1K spaces. If accessing address has over 1K, then the address will map to physical 1K memories, i.e. 1K+M will be mapped to M. A NOP at the reset vector location will cause a restart at address 000h. A simple map to induce illustrate ROM organization is shown in figures 5-1.

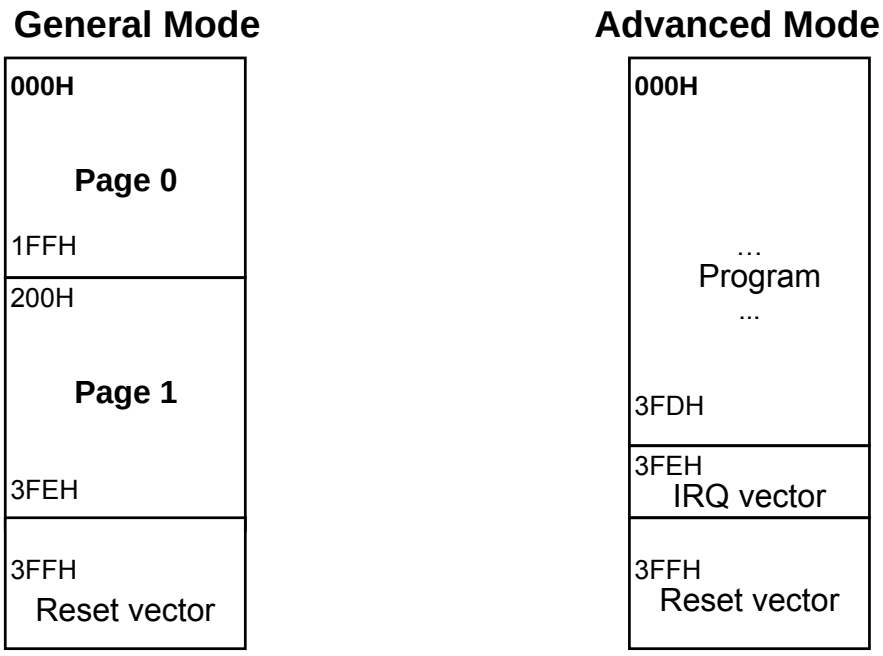


Figure 6-1 The ROM Organization

TM58PE10 only provide IRQ function in advanced mode. In this mode, the address 3FEH is reserved for IRQ vector. User can operate advanced mode by setting configuration word. The configuration word is located 800H, shown in figure 6-2.

<table>
<tr><td colspan="6">Configuration Word</td></tr>
<tr><td>Bit</td><td>Symbol</td><td colspan="4">Description</td></tr>
<tr><td rowspan="5">1~0</td><td rowspan="5">FOSC1
|
FOSC0</td><td>Bit [1]</td><td>Bit [0]</td><td>OSC Type</td><td>Resonance Frequency</td></tr>
<tr><td>0</td><td>0</td><td>LP (low speed)</td><td>32~200K Hz</td></tr>
<tr><td>0</td><td>1</td><td>NT(Normal speed)</td><td>200K~10M Hz</td></tr>
<tr><td>1</td><td>0</td><td>HS (high speed)</td><td>10~20M Hz</td></tr>
<tr><td>1</td><td>1</td><td>External RC</td><td>32K ~ 20M Hz (VDD=5V)</td></tr>
<tr><td>2</td><td>WDTE</td><td colspan="4">WDTE: Watchdog enable/disable control
1: WDT enable
0: WDT disable</td></tr>
<tr><td>3</td><td>CPT</td><td colspan="4">CPT: Code Protection bit
1: OFF
0: ON</td></tr>
<tr><td>4</td><td>TYPE</td><td colspan="4">TYPE: Select operating mode
1: Advanced mode
0: General mode</td></tr>
<tr><td rowspan="5">6~5</td><td rowspan="5">LV1~LV0</td><td>LV1</td><td>LV0</td><td colspan="2">Detect voltage</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">4V</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">Unimplemented</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">2.2V</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Don’t use</td></tr>
<tr><td>7</td><td>RESETB0</td><td colspan="4">RESETB0: External Reset Pin 1 (In General mode only set =0)
0: PA0 /RESETB0/INT0 be Normal I/O Pin
1: PA0 /RESETB0/INT0 be system reset Pin</td></tr>
<tr><td>8</td><td>RESETB1</td><td colspan="4">RESETB1: External Reset Pin 2 (In General mode only set =1)
0: PA5/RESETB1/INT1 be Input Pin
1: PA5/RESETB1/INT1 be system reset Pin</td></tr>
<tr><td>9</td><td>IOC</td><td colspan="4">IOC: OSC1, OSC2 I/O Control (In General mode only set =0)
0: OSC1, OSC2 be clock Pin
1: OSC1, OSC2 be I/O Pin</td></tr>
<tr><td>10</td><td>INRC</td><td colspan="4">INRC: Internal RC (In General mode only set =0)
0: Don’t use Internal RC clock
1: Use Internal RC clock</td></tr>
</table>

11	AUP	AUP : Auto Update Page (In General mode only set =0) 0: Disable auto update page in Advance mode 1: Enable auto update page in Advance mode

Figure 6-2 The Configuration Word

6.2 Data memory

Data memory is composed of special function registers and general-purpose ram. The size of data memory is not stationary; it depends on bit 4 of configuration word (general or advanced mode).

6.2.1 General Mode

In general mode, TM58PE10 has 25 general-purpose registers. The special function registers include the program counter (PC), the timer (TMR0) register, the status register, the bank select register (BSR), and the I/O port registers (PORTA, PORTB). Furthermore, TM58PE10 has 3 auxiliary registers that include indirect addressing register (IAR), the select register (Select) and the I/O direction register (IODIR). The register map of general mode is shown in figure 6-3.

	Bank0
00H	IAR
01H	TMR0
02H	PC
03H	STATUS
04H	BSR
05H	PORTA
06H	PORTB
9+16=25	General Purpose Register 07 H – 0F H
	General Purpose Register 10 H -1F H

Figure 6-3 The Register Map of General Mode

A. The IAR (indirect addressing register) is not a physical register and is used to assist BSR with indirect addressing. Any instruction attempts to access IAR actually mapping to another address that is pointed by BSR. Since IAR is not a material circuit, user reads IAR itself (BSR=00H) will always return 00h at data bus. Writing to IAR itself will like NOP.

B. Select register is used to control WDT and TMR0. It has not assigned a specific address in data memory and can only set control bits by “select” instruction, i.e. it is write-only register. The content of accumulator will be sent to the select register by executing the “select” instruction. If select register has never set by program, its default value is 3FH. We drew Figure 6-4 to explain how to set select register.

<table>
<tr><td colspan="7">Control register SELECT</td></tr>
<tr><td>Bit</td><td>Symbol</td><td colspan="5">Description</td></tr>
<tr><td rowspan="9">2~0</td><td rowspan="9">PS2~PS0</td><td>PS2</td><td>PS1</td><td>PS0</td><td>TMR0 rate</td><td>WDT rate</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1:2</td><td>1:1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1:4</td><td>1:2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1:8</td><td>1:4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1:16</td><td>1:8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1:32</td><td>1:16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1:64</td><td>1:32</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1:128</td><td>1:64</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1:256</td><td>1:128</td></tr>
<tr><td>3</td><td>PSA</td><td colspan="5">PSA: Prescaler assignment bit
1: Prescaler assigned to WDT
0: Prescaler assigned to TMR0</td></tr>
<tr><td>4</td><td>EDGE0</td><td colspan="5">EDGE0: TMR0 source signal edge control bit
1:increment when H→L transition on external clock
0:increment when L→H transition on external clock</td></tr>
<tr><td>5</td><td>SUR0</td><td colspan="5">SUR0: TMR0 clock source bit
1: External clock input
0: (Internal clock)/4 or internal instruction cycle</td></tr>
<tr><td>6~7</td><td>----</td><td colspan="5">Unimplemented</td></tr>
</table>

Figure 6-4 Select Register

C. The I/O Direction control register is similar to the Select register that is write-only register. To set an I/O port pin as input, the corresponding direction control bit must be high. Similarly, the zero represents output. Any direction control bit can be programmed individually as input or output by using IODIR instruction. If the register is not programmed, then all I/O ports always keep input mode.

- PC (program counter, 02H) is a 10-bit wide binary counter and increases itself for every instruction cycle, except the following instructions.
  1. call, goto, lgoto and lcall: the label will move to PC
  2. retla, reti and ret: the top value of stack will pop to PC

- Incrementing PC when it changes to the next higher page. It should be noted that the page select bits in the status register would not be changed synchronously. The following Goto, Call, MOVAM PC or ADDAM PC instruction will return to the previous page, unless the page select bits have been updated in program. In order to reduce the complexity of programming. TM58PE10 provides 2 instructions to facilitate subroutine call and branch handling which are LCALL and LGOTO. LCALL and LGOTO can address to anywhere in the ROM. However the page select bits will keep default value. If the program counter register is written then system will load page select register default value to high address. System will go the wrong address. See example on Figure 6-5-3.

- The attached operands of CALL and GOTO are 8-bit and 9-bit respectively, and so need extra bits (page select bits) to address whole memory. However, LCALL and LGOTO have 10-bit wide operands that are easy to address the total ROM space. Page select bits in control register STATUS (03H) bit [6:5] function in advance mode will be described in section 7.3.

- TMR0 is 8-bit wide binary counter/timer. This register increases by an external signal edge applied to EXT_CLK pin, or by internal instruction cycle. It has the following features.
  A. Readable and writeable
  B. Synchronize with 2 internal clocks
  C. Can use programmable prescaler by setting select register

The other details will be described in follow-up chapter.

- Status register contains page select bits, time out bit, power down bit and the status bits of ALU. Please note that $\overline{TO}$ and $\overline{PD}$ are controlled by hardware and unchangeable by program.
-

<table>
<tr><td colspan="4">Control register STATUS (03H)</td></tr>
<tr><td>Bit</td><td>Symbol</td><td colspan="2">Description</td></tr>
<tr><td rowspan="3">0</td><td rowspan="3">C</td><td colspan="2">Carry and $\overline{Borrow}$ bit</td></tr>
<tr><td>ADD instruction</td><td>SUB instruction</td></tr>
<tr><td>1: a carry occurred from the MSB
0: no carry</td><td>1: no borrow (Note1)
0: a borrow occurred from the MSB</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">DC</td><td colspan="2">Nibble Carry and Nibble $\overline{Borrow}$ bit</td></tr>
<tr><td>ADD instruction</td><td>SUB instruction</td></tr>
<tr><td>1: a carry from the low nibble bits of the result occurred
0: no carry</td><td>1: no borrow
0: a borrow from the low nibble bits of the result occurred</td></tr>
<tr><td>2</td><td>Z</td><td colspan="2">Zero bit:
1: the result of a logic operation is zero
0: the result of a logic operation is not zero</td></tr>
<tr><td>3</td><td>$\overline{PD}$</td><td colspan="2">Power down flag bit: (Note2)
1: after power-on or by the CLRWDT instruction
0: execute SLEEP instruction</td></tr>
<tr><td>4</td><td>$\overline{TO}$</td><td colspan="2">Time out flag bit: (Note2)
1: after power-on or by the CLRWDT or SLEEP instruction
0: Occur WDT time-overflow</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SA0
(A9)</td><td></td><td>Page Location</td></tr>
<tr><td>0
1</td><td>Page0 (000H~1FFH)
Page1 (200H~3FFH)</td></tr>
<tr><td>6</td><td>A8</td><td colspan="2">General mode always = “0 “, Advance mode can be set.</td></tr>
<tr><td>7</td><td>----</td><td colspan="2">Unimplemented</td></tr>
<tr><td colspan="2">Bit [5] Bit [6]
SA0 (A9) A8</td><td colspan="2"><u>Advance mode use only</u></td></tr>
<tr><td colspan="2">0 0
0 1
1 0
1 1</td><td colspan="2">Page0 (OTP mapping = 000H ~ 0FFH)
Page1 (OTP mapping = 100H ~ 1FFH)
Page2 (OTP mapping = 200H ~ 2FFH)
Page3 (OTP mapping = 300H ~ 3FFH)</td></tr>
</table>

Figure 6-5 Status Register

Note1: A SUB instruction is executed by adding the 2's complement of the subtrahend, so C = 1 represents positive result. The Figure 6-5-1 show the relation between C-bit and borrow.

B0H－50H										50H－B0H									
	C	B7	B6	B5	B4	B3	B2	B1	B0		C	B7	B6	B5	B4	B3	B2	B1	B0
＋ ＝	 1	1 1 0	0 0 1	1 1 1	1 1 0	0 0 0	0 0 0	0 0 0	0 0 0	＋ ＝	 0	0 0 1	1 1 0	0 0 1	1 1 0	0 0 0	0 0 0	0 0 0	0 0 0

Figure 6-5-1

Note2: The $\overline{TO}$ and $\overline{PD}$ bits are active low that can be used to determine different causes of reset. The Figure 6-5-2 illustrates the value of $\overline{TO}$ and $\overline{PD}$ after the relative reset events.

$\overline{TO}$	$\overline{PD}$	Reset Event
0	0	WDT time out from sleep mode
0	1	WDT time out from normal mode
1	0	Input a 'low" at RESETB0, RESETB1 from sleep mode
1	1	Power on reset
Unchanged	Unchanged	Input a "low" at RESETB0, RESETB1 from normal mode

Figure 6-5-2

Example: Used Lcall , Lgoto in general mode may take care of page select register.

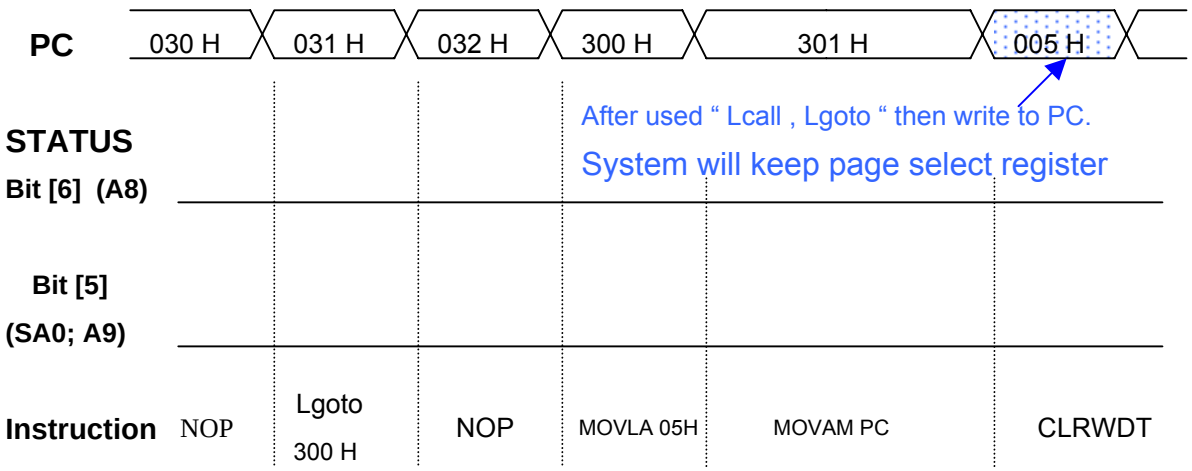


Figure 6-5-3 Use "Lgoto" instruction in general mode.

BSR (bank select register) is associated with IAR to indirectly access the data memory. The BSR<4:0> bits are used to select data memory addresses 00h to 1Fh (Bank0). The addressing map is shown in Figure 6-6.

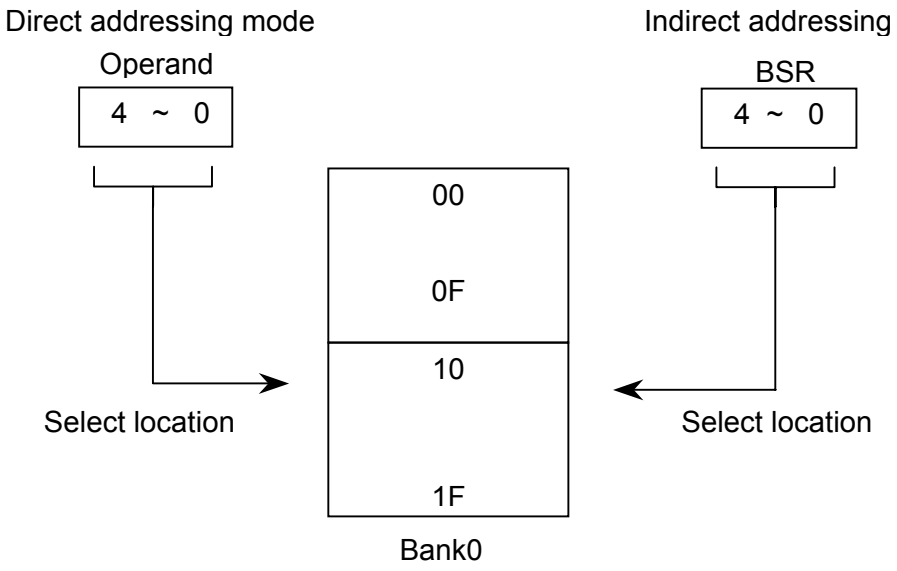


Figure 6-6 The Direct and Indirect Addressing Map

- Port A~B are programmable I/O ports. Please note that read I/O instruction always read the I/O pin even though the pin is output mode. On reset, all I/O pins were set as input mode until IODIR has been changed.

6.2.2 Advanced mode

In advanced mode, we provide IRQ, convenient wake up functions and flexible addressing mode. In addition to extend data memory, we increase 9 extra registers to support IRQ, wake_up, Timer1 and Timer2. This section will introduce these increased control registers and characteristics. The data memory map of advanced mode and the addressing map are shown in figure 6-7 and figure 6-8 respectively.

Advanced mode (Type=1)

<table>
<tr><td></td><td>00~1F</td><td></td><td>20~3F</td><td></td><td>40~5F</td></tr>
<tr><td>00H</td><td>IAR</td><td>20H</td><td>PULL-Hi</td><td>40H</td><td>WAKE_UP</td></tr>
<tr><td>01H</td><td>TMR0</td><td>21H</td><td>IRQM</td><td rowspan="8" colspan="2">Unimplemented</td></tr>
<tr><td>02H</td><td>PC</td><td>22H</td><td>IRQF</td></tr>
<tr><td>03H</td><td>STATUS</td><td>23H</td><td>WDTSEL</td></tr>
<tr><td>04H</td><td>BSR</td><td>24H</td><td>TMR1 Control</td></tr>
<tr><td>05H</td><td>PORTA</td><td>25H</td><td>TMR2 Control</td></tr>
<tr><td>06H</td><td>PORTB</td><td>26H</td><td>TMR1 Preload</td></tr>
<tr><td rowspan="2">9+16
= 25</td><td rowspan="2">General Purpose Register
07H - 0FH</td><td>27H</td><td>TMR2 Preload</td></tr>
<tr><td rowspan="2">8+16
= 24</td><td>General Purpose Register
28H - 2FH</td></tr>
<tr><td>General Purpose Register
10H - 1FH</td><td>General Purpose Register
30H - 3FH</td></tr>
</table>

Figure 6-7 The Data Memory Map of Advanced Mode

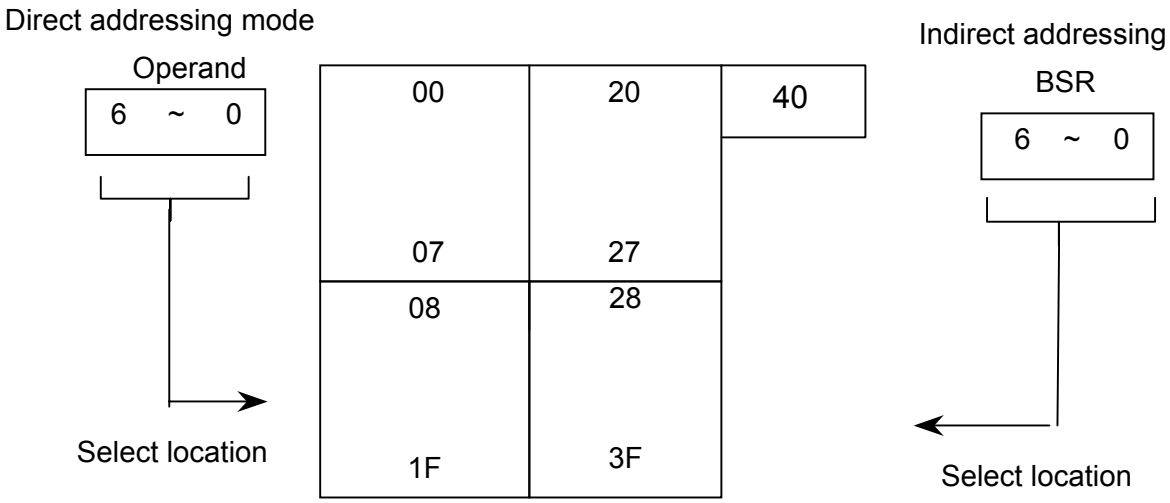


Figure 6-8 The Direct and Indirect Addressing Map

In advanced mode, we locate the increased 24 general-purpose registers on 28~3F which shown in Fig 6-7. The IRQ and the Wakeup control registers (PULL_Hi, IRQM, IRQF and WAKE_UP) are assigned to 20H, 21H, 22H and 40H respectively. In advanced mode, TM58PE10 allows 7-bit wide operand to access ram, operand<6:0> can address 00H ~ 40H directly. It doesn't need bank select bits, and reduces the complexity of programming.

- Pull-High register (PULL-Hi---20H) if (PUH [N]=1) and only if (Port B Bit [N] as input pin); [N]=7~0, then PortB Bit[N] will PULL-Hi. See Figure 6-9 PULL-Hi Register

Control register PULL-Hi (20H)		
Bit	Symbol	Description
7~0	PUH [7]~PUH [0]	Pull High Port B bit7 ~ bit0: 0: disable pull-hi function. 1: Enable Pull High bit (Bit [7] ~ Bit [0])

Figure 6-9 PULL-Hi Register

- The wakeup control register (WAKE_UP; 40H) is used to set watchdog enable and distinguish between external wake-up signal, EXT_CLK I/O control and IRQ. WUE bit control external wake-up function. In TM58PE10 wakeup operation in PortB be input pin and pin change wakeup; see page 22. On reset, all bits are defined as ”0”; except for bit [5] “RTCEN” defined as ”0” that can be programming by software. The scheme of WAKE_UP register is shown in Fig 6-10.

Control register WAKE_UP (40H)		
Bit	Symbol	Description
7	WDTS	Watch Dog Timer Software Control bit: TM58PE10 has 2 WDT control bits (WDTE and WDTS), WDTE is set in configuration word by hardware and WDTS is set in control register by software. If WDTS is valid only if WDTE has been set, i.e. WDTE has higher priority than WDTS. 1: enable 0: disable
6	WUE	Wake Up Enable bit: 1: enable external wake-up function 0: disable external wake-up function
5	RTCEN	EXT_CLK be I/O Pin Enable bit: 1: set EXT_CLK/PA4 as a normal clock pin 0: set EXT_CLK/PA4 as a bi-directional I/O pin *(default value)*
4~2	----	Unimplemented read as “0“
1	EIS1	External Interrupt Select1: 1: set RESETB1/PA5/INT1 as an external IRQ pin (Note3) 0: set RESETB1/PA5/INT1 as a Input pin
0	EIS0	External Interrupt Select0: 1: set PA0/RESETB0/INT0 as an external IRQ pin (Note3) 0: set PA0/RESETB0/INT0 as a bi-directional I/O pin

Figure 6-10 WAKE_UP Register

Note3: The IRQ must execute at normal mode. If an IRQ is occurred at sleep mode, then the IRQ routine will be performed until this chip has woken by external wake up signal. Other wake methods include (1) power on reset, (2) external reset and (3)

WDT overflow (if enabled), the foregoing cases mean the IRQ ought to be abolished.

- The Interrupt Mask register and Interrupt Flag register are used to control IRQ handling. A TM58PE10 support TMR0, TMR1, TMR2 and two external interrupt (INT0, INT1), but nest-interrupt is not allowed. The schemes of the interrupt mask register and the interrupt flag register are shown in Fig 6-10 and 6-11, respectively.

Control register IRQM (21H)		
Bit	Symbol	Description
7	INTM	Global enable bit: The bit has higher priority than any interrupt enable signal. 1: enable 0: disable By the way, when system occur interrupt the INTM will be cleared by hardware and RETI instruction will set INTM as '1'.
6	----	Unimplemented
5	TMR2M	TMR2 Interrupt enable: 1:Enable Interrupt 0:Disable Interrupt
4	TMR1M	TMR1 Interrupt enable: 1:Enable Interrupt 0:Disable Interrupt
3	----	Unimplemented
2	EXINTM1	External Interrupt enable PA5/RESETB1/INT1: 1:Enable Interrupt 0:Disable Interrupt
1	EXINTM0	External Interrupt enable PA0/RESETB0/INT0: 1:Enable Interrupt 0:Disable Interrupt
0	TMR0M	TMR0 Interrupt enable: 1:Enable Interrupt 0:Disable Interrupt

Figure 6-10 Interrupt Mask register

Control register IRQF (22H)		
Bit	Symbol	Description
7~6	----	Unimplemented
5	TMR2F	TMR2 interrupt flag: 1: The TMR2 counter overflow generates an interrupt request.
4	TMR1F	TMR1 interrupt flag: 1: The TMR1 counter overflow generates an interrupt request.
3	----	Unimplemented
2	EXINTF1	External interrupt flag: 1: the External interrupt be requested by the external interface PA5/RESETB1/INT1 (Note4)
1	EXINTF0	External interrupt flag: 1: the External interrupt be requested by the external interface PA0/RESETB0/INT0 (Note4)
0	TMR0F	TMR0 interrupt flag: 1: The TMR0 counter overflow generates an interrupt request.

Figure 6-11 Interrupt Flag register

Note 4: Both interrupt flags are set by hardware; software can only clear flags. It is useless that attempt writing '1' to flag.

- If user don't setting perscaler rate to WDT, the default base period is 16mS . In TM58PE10 advance mode, user can select different base period by setting WDTSEL register (23H). Program will run following the sleep instruction after wakeup by portB in sleep mode. There will be a response time from wakeup to program running (see the illustrated waveform below). The response time is affected by WDT base period and user can set different response time by setting WDT base period.

Default response time value is 16mS. See in Figure 6-12 and example in following text.

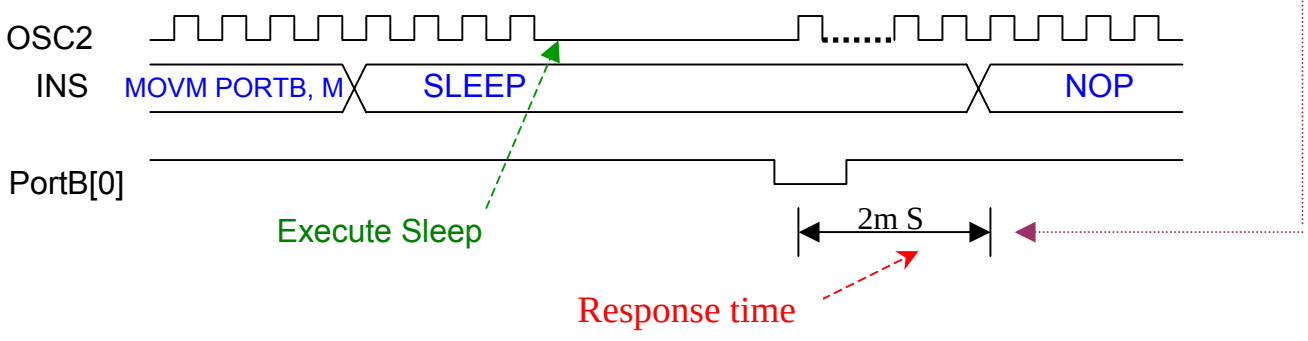
Control register WDTSEL (23H)		
Bit	Symbol	Description
7~2	----	Unimplemented
Bit [1]	Bit [0]	Wakeup response time (Base on Watch Dog Timer period)
S1	S0	
0	0	1mS
0	1	4mS
1	0	8mS
1	1	16mS (default value)

Figure 6-12 WDTSEL register

Example: How to reduce wakeup response time

```
MOVLA    40H
MOVAM    WAKE_UP
 ;  Set wakeup enable
MOVLA     01H
IODIR      PORTB
MOVAM     PULL-Hi
 ; Set PB [0] input pin and pull-high
MOVLA    00H
MOVAM   WDTSEL
; Set WDTSEL base period=1ms ----------
                                        MOVLA 09H
                                         SELECT
                                        ; Prescaler rate = 1:2 = 2ms

                                        CLRWDT
                                        MOVM    PORTB, M
                                        ; Read PortB to determine Pin status
                                         SLEEP
                                         NOP
```



- In this section we describe Timer1 and Timer2 Control register. Some detailed function description in section 7.3. Timer1 and Timer2 register setting need consider about Configuration Word. That can make Timer1 and Timer2 operation more correctly.

<table>
<tr><th colspan="6">Control register TMR1 Control (24H)</th></tr>
<tr><th>Bit</th><th>Symbol</th><th colspan="4">Description</th></tr>
<tr><td>7</td><td>TMR1EN</td><td colspan="4">Timer1 count Enable bit
1: Timer1 count enable
0: Timer1 count disable</td></tr>
<tr><td>6</td><td>LOAD</td><td colspan="4">Timer1 data load mode
1: Counter, when data write to Timer1 data register (26H)
Timer1 count value is written immediately. (Default value)
0: Preload, when data write to Timer1 data register (26H),
Waiting Timer1count overflow then load data.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SUR1</td><td colspan="2">SUR1 SUR0</td><td colspan="2">Timer1 source
(Refer to example 7.4.1 at page 33)</td></tr>
<tr><td rowspan="2">0 0</td><td colspan="2" rowspan="2">From System CLK (only Internal RC or External RC) (Note5)</td></tr>
<tr><td>4</td><td>SUR0</td></tr>
<tr><td></td><td></td><td>0 1
1 0
1 1</td><td colspan="2">From EXT_CLK
From Timer2 (connect to be 16 bit timer)
Unimplemented</td></tr>
<tr><td>3</td><td>EDGE1</td><td colspan="4">EDGE1: TMR1 source from EXT_CLK signal edge control bit
1:increment when EXT_CLK H→L transition
0:increment when EXT_CLK L→H transition</td></tr>
<tr><td rowspan="2">2~0</td><td rowspan="2">PS2~PS0</td><td>PS2</td><td>PS1</td><td>PS0</td><td>Timer1 Prescaler rate</td></tr>
<tr><td>0
0
0
0
1
1
1
1</td><td>0
0
1
1
0
0
1
1</td><td>0
1
0
1
0
1
0
1</td><td>1: 1
1: 2
1: 4
1: 8
1: 16
1: 32
1: 64
1: 128</td></tr>
</table>

Figure 6-13 Timer1 Control register

<table>
<tr><td colspan="6">Control register TMR2 Control (25H)</td></tr>
<tr><td>Bit</td><td>Symbol</td><td colspan="4">Description</td></tr>
<tr><td>7</td><td>TMR2EN</td><td colspan="4">Timer2 count Enable bit
1: Timer2 count enable
0: Timer2 count disable</td></tr>
<tr><td>6</td><td>LOAD</td><td colspan="4">Timer2 data load mode
1:Counter, when data write to Timer2 data register (27H)
Timer2 count value is written immediately. (Default value)
0: Preload, when data write to Timer2 data register (27H),
Waiting Timer2count overflow then load data.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SUR1</td><td>SUR1</td><td>SUR0</td><td colspan="2">Timer2 source
(Refer to example 7.4.1 at page 33)</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">From System CLK (Only Crystal mode) (Note5)</td></tr>
<tr><td>4</td><td>SUR0</td><td>0
1
1</td><td>1
0
1</td><td colspan="2">From EXT_CLK
From Timer1 (connect to be 16 bit timer)
Unimplemented</td></tr>
<tr><td>3</td><td>EDGE2</td><td colspan="4">EDGE2: TMR2 source from EXT_CLK signal edge control bit
1:increment when EXT_CLK H→ L transition
0:increment when EXT_CLK L→ H transition</td></tr>
<tr><td>2~0</td><td>PS2~PS0</td><td>PS2</td><td>PS1</td><td>PS0</td><td>Timer2 Prescaler rate</td></tr>
<tr><td></td><td></td><td>0
0
0
0
1
1
1
1</td><td>0
0
1
1
0
0
1
1</td><td>0
1
0
1
0
1
0
1</td><td>1: 1
1: 2
1: 4
1: 8
1: 16
1: 32
1: 64
1: 128</td></tr>
</table>

Figure 6-14 Timer2 Control register

Note 5: Configuration Word bits [1:0] can only select one operate mode, which is either crystal mode (HS, XT and LP) or external RC mode. *So Timer1 and Timer2 can't adopt Crystal and External RC at the same time*.

Control register TMR1, TMR2 data register (26H, 27H)		
Bit	Symbol	Description
7~0	D7~D0	Timer1 and Timer2 data register. Default data D7~ D0 = FFH

Figure 6-15 Timer1 and Timer2 data register

The debounce time is the interval that must pass before a second pressing of a key is accepted. User can set this interval with the delay routine (See Example A).

Example A :Key bounce

```
interrup
;---------------------------------------
   btmss   irqf,1       ;; if external IRQ(INT0)?
   lgoto   int_end
int_nt1:                ;; filter out key begin bounce
   btmsc   ra,0
   lgoto   int_nt1
int_loop1:              ;; filter out key end bounce
   call    delay        ;; worse case 30ms
   btmss   ra,0
   lgoto   int_loop1

   call    delay        ;; such as 30ms
   btmss   ra,0
   lgoto   int_loop1
;-------------------------------------
   bcm     irqf,1
int_end:
   reti
```

7. Functional Description

7.1 TMR0 and Watchdog timer

Fig. 7-1 shows the block diagram of the TMR0/WDT prescaler. As shown in the figure, the prescaler register can be a pre-scaler for TMR0 or be a post-scaler for WDT.

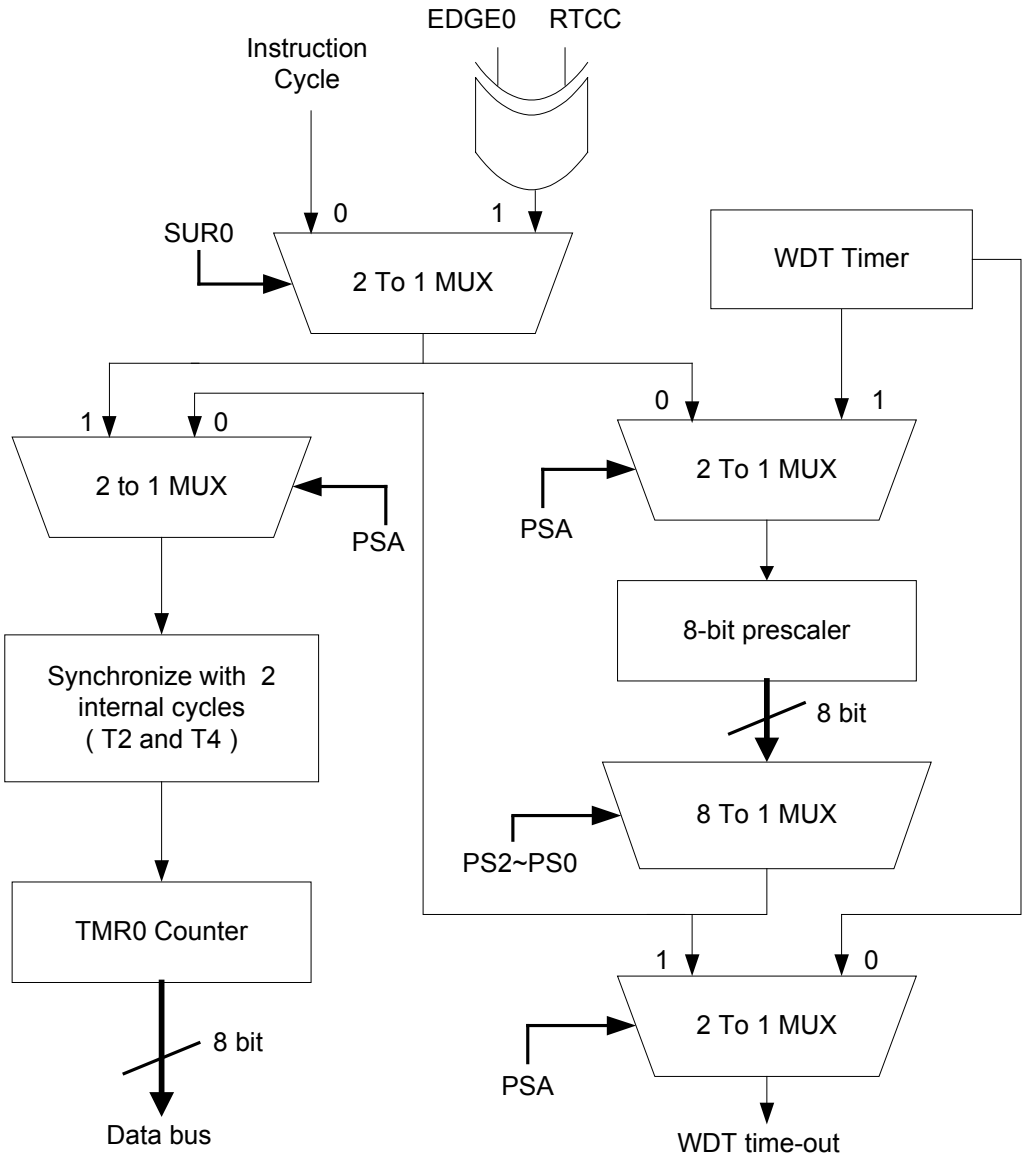


Figure 7-1 Block Diagram of the TMR0/WDT Prescaler

The TMR0 is an 8-bit timer/counter. The clock source of TMR0 can come from the instruction clock or the external clock.

A. To select the instruction clock, the SUR0 bit of the select register should be clear. When no prescaler is used, TMR0 will increase by 1 at every instruction cycle.

B. To select the external clock, the SUR0 bit of the select register should be set. In this mode, TMR0 relies on the EDGE0 bit to determine that TMR0 is increased by 1 at every falling or rising edge. When an external clock is used for TMR0, a problem must be noted that the external clock synchronizes with internal clock. TM58PE10 synchronizes external clock by sampling internal clock at T2 and T4. If external pulse is smaller than 2 internal cycles, the pulse maybe ignored. Therefore, the external clock must keep stable state (high or low) for at least 2 internal cycles.

The WDT counter is an 8-bit binary counter. The clock source of WDT is provided by an independent on-chip RC oscillator that does not need any external clock. Therefore, the WDT will keep counting even if the chip has slept already. A WDT time-out will restart system and set the time-out flag bit (bit4 of status register) as “0”. The WDT time-out period vary with temperature, power voltage and process. This period can be improved via the prescaler. The maximum division ratio can up to 1:128 by setting PS2~PS0 bits of select register as “111”.

The prescaler can be assigned to either the TMR0 or the WDT via the PSA bit of select register. Note that either WDT or TMR0 cannot employ the prescaler simultaneously. When the prescaler is assigned to WDT, “CLRWDT” and “SLEEP” instruction will clear the prescaler and the WDT. When the prescaler is assigned to TMR0, the prescaler will be cleared by any instruction that writes to TMR0.

7.2 Reset

TM58PE10 may be reset by one of the following conditions:

(1) Power-on.

(2) Low voltage reset (circuit protection), refer to electrical characteristic.

(3) RESETB1/VPP/PA5/INT1 or PA0/RESETB0/INT0 (if be set as reset pin) input a negative pulse.

(4) WDT timer out reset (if enabled).

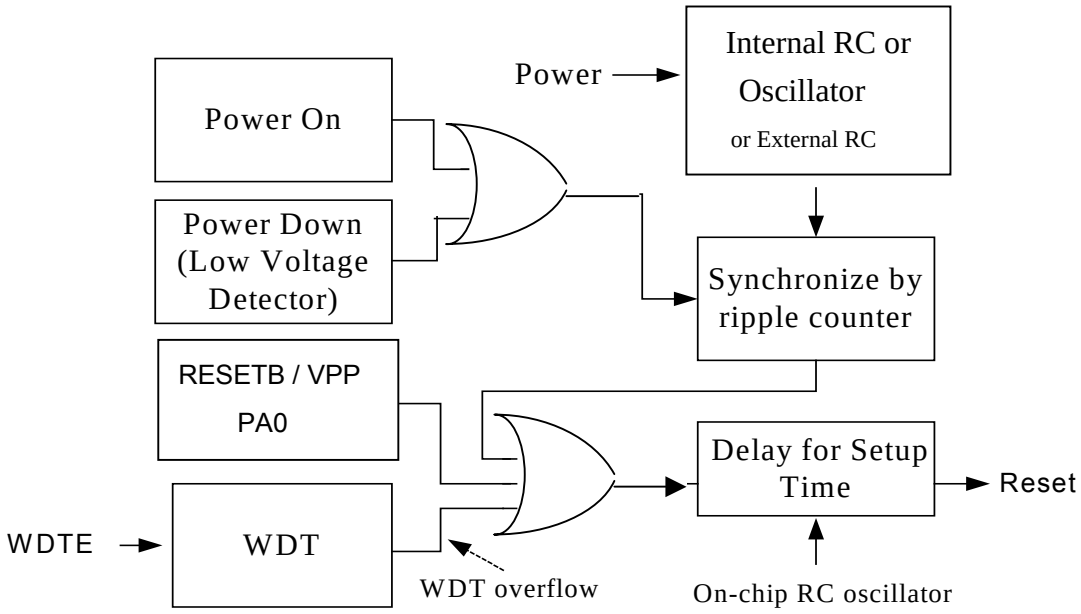


Figure 7-2 Scheme of the Reset Controller

As shown in the figure 7-2, four reset conditions are listed. The power-down event will cause TM58PE10 to reset which the voltage ranges is according to the bit6~bit5 in the configuration word. This condition is used to protect chip in deficient power environment. The voltage ranges of power-down are defined in electrical characteristics. Furthermore, the ranges may be influenced by process and temperature variations. In general, we call the first two reset-cases as cold reset. The cold reset time may be too short for slow crystals and RC oscillators that require much longer than setup time (note6) to oscillate. In order to insure the system is correct, the events should be synchronized with system clock.

Note6: the setup time is approximately 16ms that will affect due to power voltage, process and temperature variations.

The last two cases are called warm reset. The different reset events will affect registers and ram. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset. These relation are listed in figure 7-3

Address	Name	Cold Reset	Warm Reset
N/A	Accumulator	xxxx xxxx	pppp pppp
N/A	IODIR	1111 1111	1111 1111
N/A	Select	----11 1111	----11 1111
00H	IAR	---- ----	---- ----
01H	TMR0	xxxx xxxx	pppp pppp
02H	PC	111 1111 1111	111 1111 1111
03H	STATUS	0001 1xxx	000? ?ppp [1]
04H	BSR (In General mode)	111x xxxx	111p pppp
04H	BSR (In Advance mode)	1xxx xxxx	1ppp pppp
05H	PORTA	0000 xxxx	0000 pppp
06H	PORTB	xxxx xxxx	pppp pppp
07H~1FH	General Purpose RAM	Xxxx xxxx	Pppp pppp
20H	PULL-Hi	0000 0000	0000 0000
21H	IRQM	0000 0000	0000 0000 [2]
22H	IRQF	0000 0000	0000 0000
23H	WDTSEL	0000 0011	0000 0011
24H	TMR1 Control	0100 0000	0100 0000
25H	TMR2 Control	0100 0000	0100 0000
26H	TMR1 Preload	1111 1111	1111 1111
27H	TMR2 Preload	1111 1111	1111 1111
28H~3FH	General Purpose RAM	Xxxx xxxx	Pppp pppp
40H	WAKE_UP	000- - -00	000- - -00

Figure 7-3 RESET CONDITIONS

X: unknown; P: previous data ; ?: value depends on condition ;
-:unimplemented and read as"0".

7.3 STATUS [6:5] (Page select bits) in advance mode

In Advance mode, system can auto update STATUS [6:5] (page select bits) by hardware or write STATUS [6:5] by software. User can use instruction " Lcall ," Lgoto ", "Ret ", "Retla " and " Reti ", it can go anywhere in OTP by hardware. Above-mentioned five instructions need two instruction cycles to operate. See operation diagram in Figure 7-4.

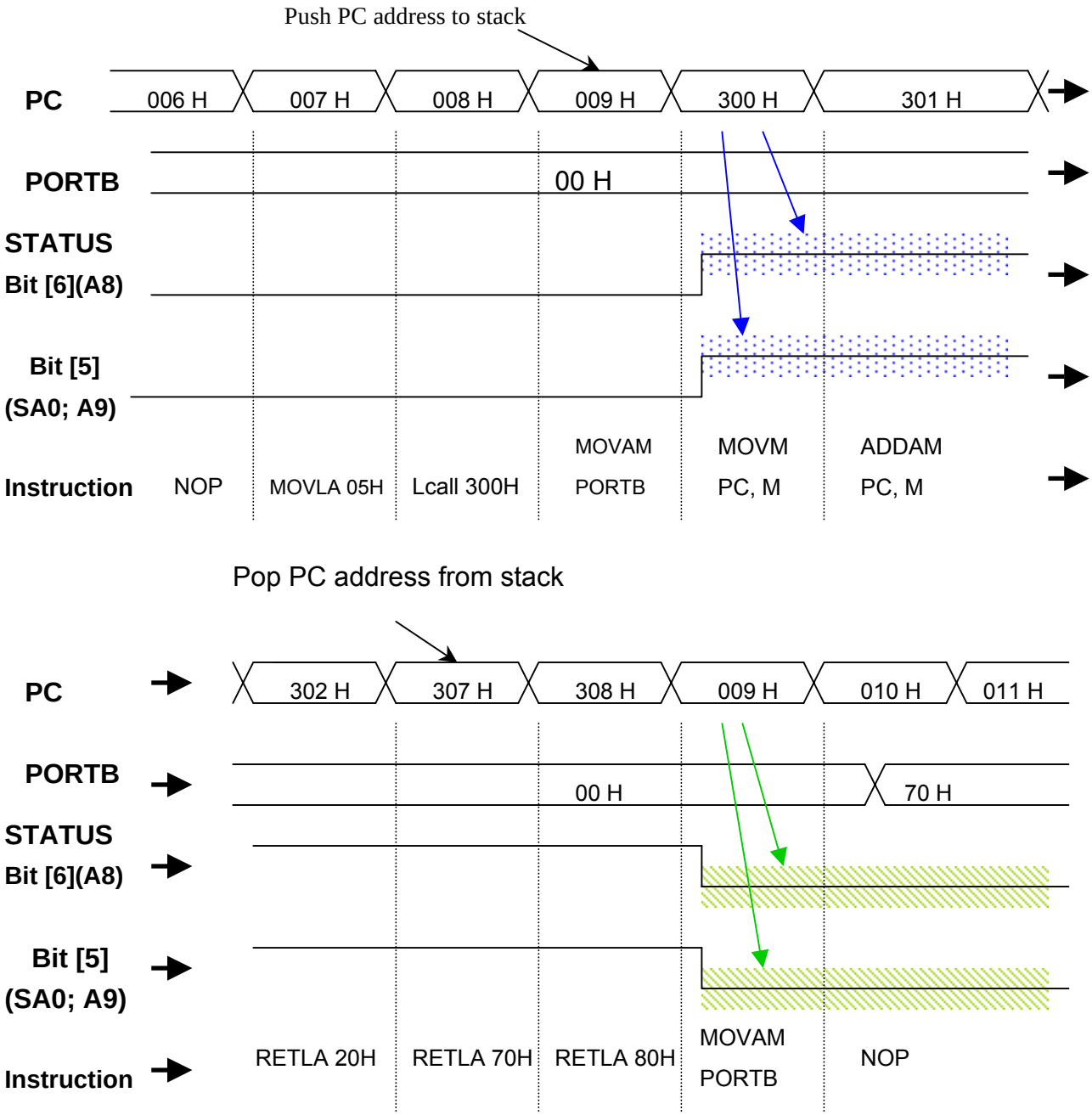


Figure 7-4 STATUS [6:5] (Page select bits) operation diagram

However user need attention occur interrupt. For example, if STATUS [6:5] default value = 00 then user write STATUS [6:5] =10 by software before occur interrupt. After occurs interrupt, system addressing to interrupt vector 3FEH. It will auto update the page select register STATUS [6:5] =11 (page3) by hardware. After finishes interrupt, stack pop PC+1 address to system, STATUS [6:5] = 00.Before occur interrupt, page select register STATUS bit [5:6] is written =10 will loss. User need take care about interrupt when you write STATUS [6:5] (page select bits) by yourself in advance mode. If user want disable auto update page function in advance mode, please set Configuration Word Bit [11] =0. In this example the page select register STATUS bit [5:6] =10 won't loss. See operation diagram in Figure 7-5.

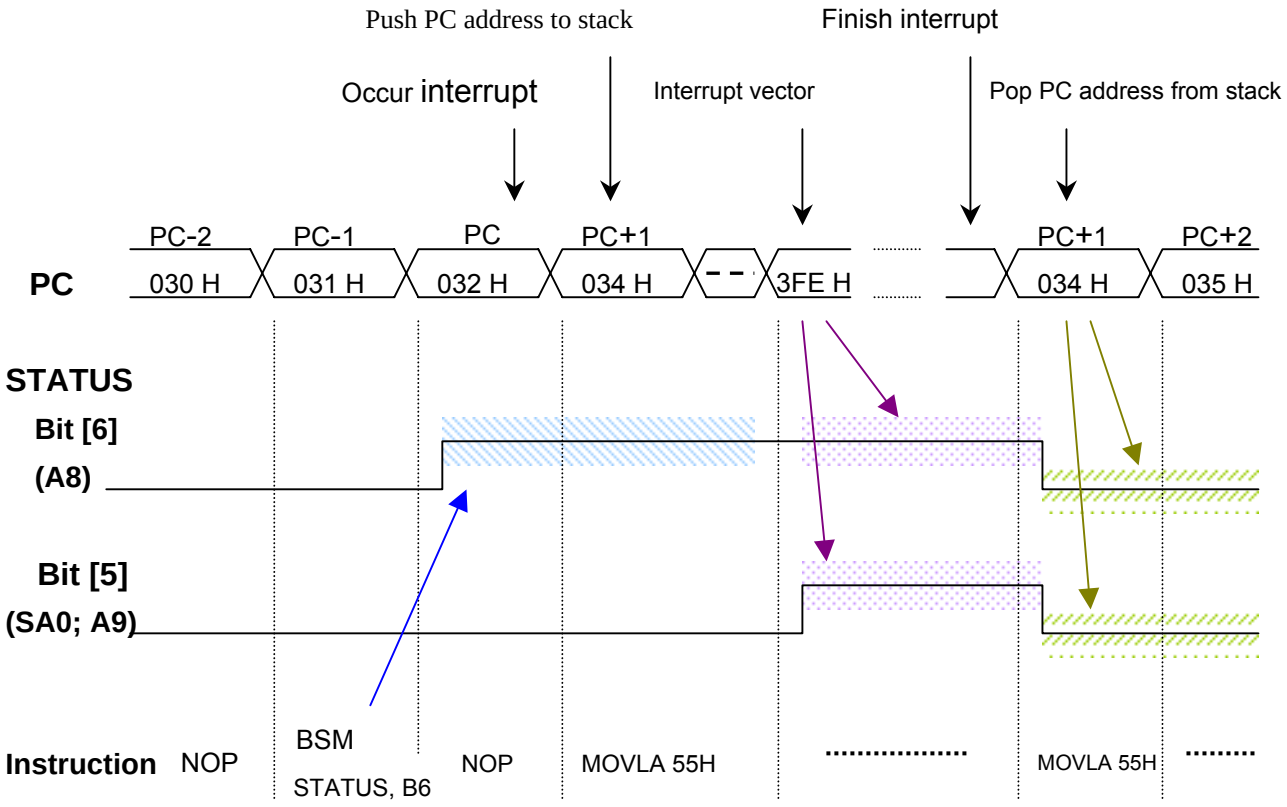


Figure 7-5 STATUS [6:5] operation with occur interrupt diagram.
When Configuration Word Bit [11] set =1.

7.4 Timer1 and Timer2

In Figure 7-6-1 shows the block diagram of the TMR1/TMR2 data register (counter / preload). Reading from TMR1/ TMR2 data register will push TMR1/ TMR2 value to accumulator. Writing to TMR1/ TMR2 data register will push accumulator value to TMR1/ TMR2, depends on data load mode. If Load mode of TMR1/ TMR2 control register has be set =1, the TMR0/ TMR2 data register will be modified immediately.

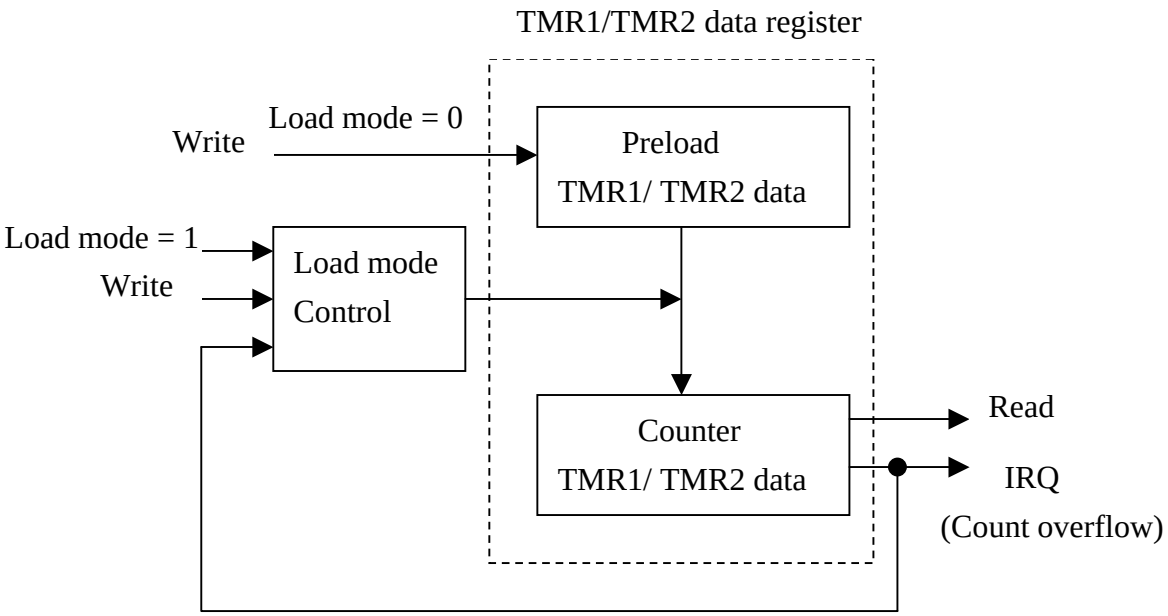


Figure 7-6-1 TMR1/TMR2 data register (counter / preload)

Figure 7-6 -2 shows the block diagram of the Timer1 and Timer2 prescaler. As show in the figure; Timer1 and Timer2 can be 8 bits X 1 countdown timer and register default value is FFH. Two timer can connect together be one 16 bits X 1 countdown timer default value is FFFFH. If user wants to use Timer1 and Timer2 in interrupt function, please don't set counter value = "00H" or "01H" avoid occur error function in timer interrupt.

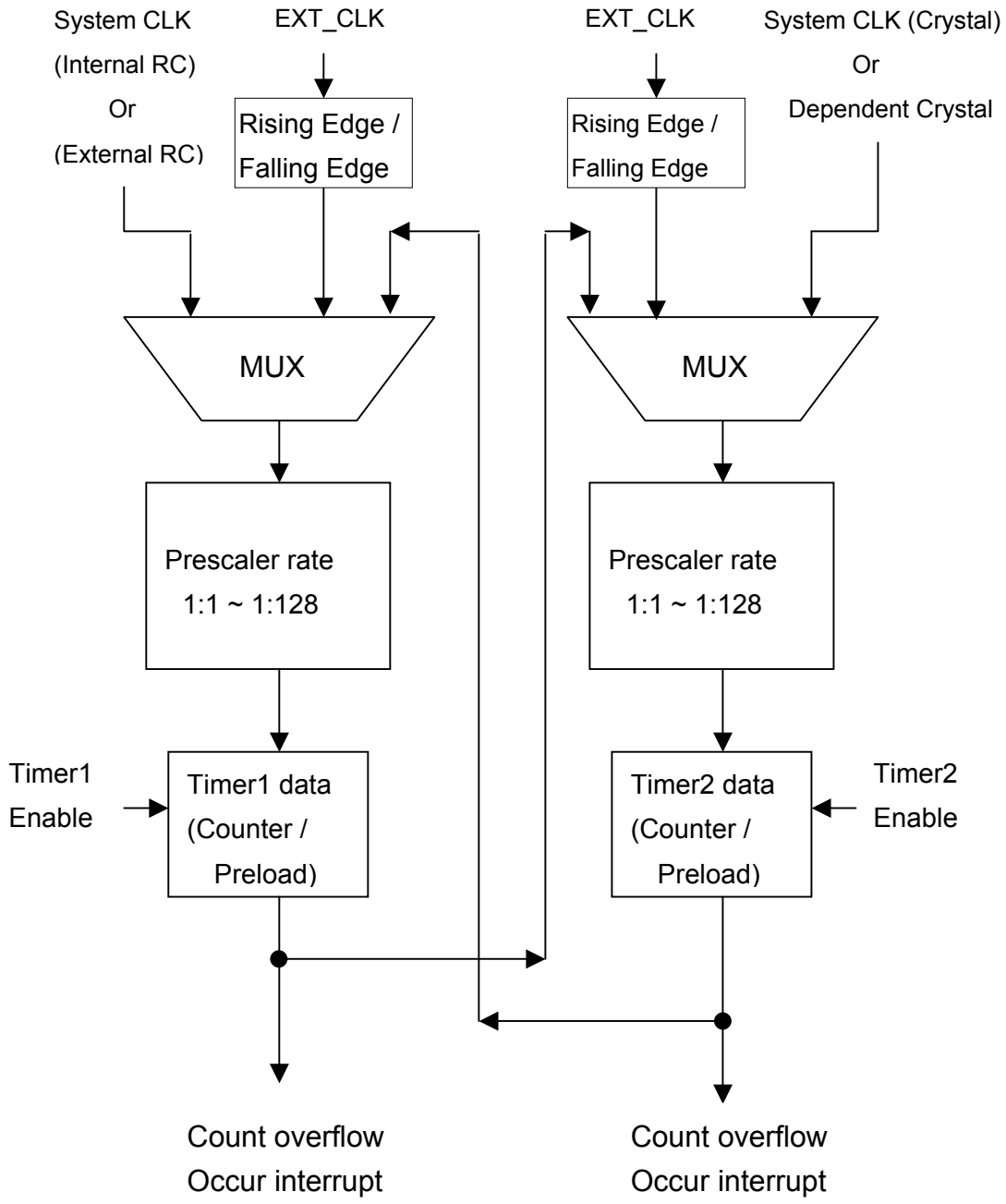


Figure 7-6-2 Block Diagram of the TMR1 and TMR2

For example, when user wants to get a 16-bit counter, source from internal RC. Timer1 is first order and Timer2 is second order. We can set Timer2 source from Timer1, connection a 16-bit counter. User can set prescaler rate in Timer1 control register, and then Timer1 clock connect to Timer2 won't do prescaler again, please set prescaler rate 1:1. The clock from Timer1 will connect to Timer2 counter directly.

TMR1 and TMR2 clock source from internal RC, External RC and Crystal. Two timer control register and Configuration Word can assemble more different function. It shows in example 7.4.1.

Example 7.4.1: How to set Configuration Word Bit [10:9] and Bit [1:0] for user?
(See Figure 7-7)

Step 1: Determine system clock from Internal RC, External RC or Crystal.
Step 2: Determine OSC1/OSC2 want to be clock pin or normal I/O pin.
Step 3: Determine what source will be used in Timer1 and Timer2.
Step 4: Set the Configuration Word Bit [10:9] and Bit [1:0] that you want.

System Clock	OSC1 OSC2 Status	Timer1 Source	Timer2 Source	Configuration Word				Operation Clock		
				SBIT [10]	SBIT [9]	SBIT [1]	SBIT [0]			
				INRC	IOC	FOSC1	FOSC0	IN_RC	Crystal	EX_RC
IN_RC	I/O	IN_RC	-----	1	1	-----	-----	V	----	----
IN_RC	Clock	IN_RC	Crystal	1	0	Crystal (HS, XT, LP)		V	V	----
Crystal	Clock	-----	Crystal	0	0	Crystal (HS, XT, LP)		----	V	----
EX_RC	Clock	EX_RC	-----	0	0	External RC		----	----	V

Figure 7-7 TMR1and TMR2 assemblies with Configuration Word
(V: used, - - -: don't used)

In Figure7-7, TMR1 and TMR2 source show "-----" also can select EXT_CLK or another TMR1, TMR2 (be 16bits X 1 timer). SBIT [10:9]=10; system clock use internal RC and TMR2 source clock use crystal, the dual clock can operate at the same time. TMR1and TMR2 control register description in Figure 6-13 and Figure 6-14.

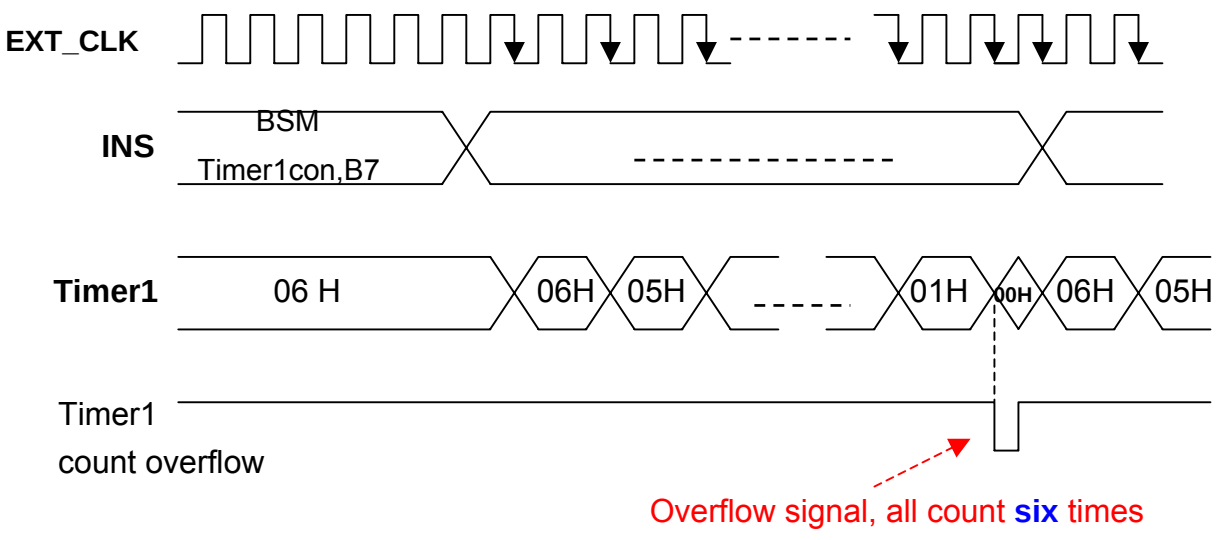
7.5 Example program for the Configuration Word , Timer1 and Timer2

Example1: Timer1 operation diagram

Timer1 source from EXT_CLK.

```
Timer1_con  EQU  24H
Timer1_pre  EQU   26H

 MOVLA  59H
MOVAM  Timer1_con ; Timer1 source from EXT_CLK (H -> L transtion)
                  ; Prescaler rate 1:2
MOVLA  06H
MOVAM  Timer1_pre ; In Timer1_con load data mode=1
                  ; Timer1 count value = 06H
                   ; Total count N times occur overflow = 6 times
BSM  Timer1_con,b7 ;
```



Example2: Dual Clock Application

Set Configuration Word Bit 10 and Bit 9= 10
We select system clock from Internal RC.
Timer1 source from Internal RC.
Timer2 source from Crystal.

```
Timer1_con EQU 24H
Timer2_con EQU 25H
Timer1_pre EQU 26H
Timer2 _pre EQU 27H

 MOVLA  40H
MOVAM  Timer1_con ; Timer1 source from Internal RC set prescaler rate 1:1

MOVLA  01H
MOVAM  Timer2_con ; Timer2 source from Crystal and prescaler rate 1:2

MOVLA  77H            ;
MOVAM  Timer1_pre ; In Timer1_con set  load data mode=1
                      ;Timer1 count value=77H

 MOVLA  50H
MOVAM  Timer2_pre ; In Timer2_con load data mode=0
                      ; Timer2 count value = FFH (default value)
                      ; Waiting “FFH” count overflow then load “50H” to Timer2

 BSM  Timer2_con,b7 ;  Timer2 countdown enable
BSM  Timer1_con,b7 ;  Timer1 countdown enable
```

Example 3

Set Configuration Word Bit 10 and Bit 9= 11

We select system clock from internal RC and OSC1/OSC2 will be I/O Pin.

Timer1 source from internal RC.

Timer2 source from Timer1 connect to be a 16 bit x 1 timer.

```
Timer1_con EQU 24H
Timer2_con EQU 25H
Timer1_pre EQU 26H
Timer2 _pre EQU 27H

 MOVLA  42H
MOVAM  Timer1_con ; Timer1 source from internal RC and prescaler rate 1:4

MOVLA  60H
MOVAM  Timer2_con ; Timer2 source from timer1 and only can set prescaler rate 1:1
                  ; connect to be 16 bit x1 timer

MOVLA  77H
MOVAM  Timer1_pre ; In Timer1_con set  load data mode=1


MOVLA  50H            ; In Timer2_con set  load data mode=1
MOVAM  Timer2_pre ;  16 bit x 1 timer value = 5077 H


BSM  Timer1_con,b7 ;  Timer1 countdown enable ( first order countdown first)
BSM  Timer2_con,b7 ;  Timer2 countdown enable ( second order countdown later)
```

Example 4

Set Configuration Word Bit 10 and Bit 9= 00

We select system clock from Crystal.

Timer2 source from Crystal.

Timer1 source from Timer2 be a 16-bit timer.

```
Timer1_con EQU 24H
Timer2_con EQU 25H
Timer1_pre EQU 26H
Timer2 _pre EQU 27H

 MOVLA  60H
MOVAM  Timer1_con ; Timer1 source from Timer2 and only can set prescaler rate 1:1

MOVLA  41H
MOVAM  Timer2_con ; Timer2 source from Crystal and prescaler rate 1:2

 MOVLA  50H
MOVAM  Timer2_pre ;

MOVLA  77H
MOVAM  Timer1_pre ;  Timer1 count value = 7750 H

 BSM Timer2_con,b7 ;  Timer2 countdown enable ( first order countdown first)
 BSM Timer1_con,b7 ;  Timer1 countdown enable ( second order countdown later)
```

Example 5

Set Configuration Word Bit 10 and Bit 9= 00

We select system clock from Crystal.

Timer1 source from EXT_CLK.

Timer2 source from Crystal.

```
Timer1_con  EQU  24H
Timer2_con  EQU  25H
Timer1_pre  EQU   26H
Timer2 _pre  EQU  27H

 MOVLA  58H
MOVAM  Timer1_con ; Timer1 source from EXT_CLK (H -> L transtion)
                  ; Prescaler rate 1:1
MOVLA  40H
MOVAM  Timer2_con ; Timer2 source from Crystal
                  ; Prescaler rate 1:1

MOVLA  77H
MOVAM  Timer1_pre ; In Timer1_con load data mode=1
                  ; Timer1 count value = 77H

MOVLA  50H
MOVAM  Timer2_pre ; In Timer2_con load data mode=1
                  ; Timer2 count value = 50H

BSM  Timer2_con,b7 ;
BSM  Timer1_con,b7 ;
```

8. Instruction Set

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	OP-code
ADDAM M, m	(M)+(acc) → (M)	1	C, DC, Z	10 0101 1MMM MMMM
ADDAM M, a	(M)+(acc) → (acc)	1	C, DC, Z	10 0101 0MMM MMMM
ANDAM M, m	(M). (acc) → (M)	1	Z	10 0100 1MMM MMMM
ANDAM M, a	(M). (acc) → (acc)	1	Z	10 0100 0MMM MMMM
ANDLA I	Literal . (acc) → (acc)	1	Z	11 1001 I III I III I
BCM M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BCM M, b1	Clear bit1 of (M)	1	None	00 1100 1MMM MMMM
BCM M, b2	Clear bit2 of (M)	1	None	00 1101 0MMM MMMM
BCM M, b3	Clear bit3 of (M)	1	None	00 1101 1MMM MMMM
BCM M, b4	Clear bit4 of (M)	1	None	00 1110 0MMM MMMM
BCM M, b5	Clear bit5 of (M)	1	None	00 1110 1MMM MMMM
BCM M, b6	Clear bit6 of (M)	1	None	00 1111 0MMM MMMM
BCM M, b7	Clear bit7 of (M)	1	None	00 1111 1MMM MMMM
BSM M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BSM M, b1	Set bit1 of (M)	1	None	00 1000 1MMM MMMM
BSM M, b2	Set bit2 of (M)	1	None	00 1001 0MMM MMMM
BSM M, b3	Set bit3 of (M)	1	None	00 1001 1MMM MMMM
BSM M, b4	Set bit4 of (M)	1	None	00 1010 0MMM MMMM
BSM M, b5	Set bit5 of (M)	1	None	00 1010 1MMM MMMM
BSM M, b6	Set bit6 of (M)	1	None	00 1011 0MMM MMMM
BSM M, b7	Set bit7 of (M)	1	None	00 1011 1MMM MMMM
BTMSC M, b0	If bit0 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTMSC M, b1	If bit1 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 1MMM MMMM
BTMSC M, b2	If bit2 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 0MMM MMMM
BTMSC M, b3	If bit3 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 1MMM MMMM
BTMSC M, b4	If bit4 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 0MMM MMMM

BTMSC M, b5	If bit5 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 1MMM MMMM
BTMSC M, b6	If bit6 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 0MMM MMMM
BTMSC M, b7	If bit7 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 1MMM MMMM
BTMSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTMSS M, b1	If bit1 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 1MMM MMMM
BTMSS M, b2	If bit2 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 0MMM MMMM
BTMSS M, b3	If bit3 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 1MMM MMMM
BTMSS M, b4	If bit4 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 0MMM MMMM
BTMSS M, b5	If bit5 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 1MMM MMMM
BTMSS M, b6	If bit6 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 0MMM MMMM
BTMSS M, b7	If bit7 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 1MMM MMMM
CALL I	Call subroutine	2	None	11 0110 I III I III
CLRA	Clear accumulator	1	Z	10 0001 0000 0000
CLRM M	Clear memory M	1	Z	10 0001 1MMM MMMM
CLRWDT	Clear watch-dog register	1	$\overline{TO}$, $\overline{PD}$	10 0000 0000 0001
COMM M, m	~(M) → (M)	1	Z	10 0010 1MMM MMMM
COMM M, a	~(M) → (acc)	1	Z	10 0010 0MMM MMMM
DECM M, m	Decrement M to M	1	Z	10 0110 1MMM MMMM
DECM M, a	(M) - 1 → (acc)	1	Z	10 0110 0MMM MMMM
DECMSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	10 0111 1MMM MMMM
DECMSZ M, a	(M) - 1 → (acc), skip if (M) = 0	1 + (skip)	None	10 0111 0MMM MMMM
GOTO I	Goto branch	2	None	11 101I III I IIII
INCM M, m	(M) + 1 → (M)	1	Z	10 1000 1MMM MMMM
INCM M, a	(M) + 1 → (acc)	1	Z	10 1000 0MMM MMMM
INCMSZ M, m	(M) + 1 → (M), skip if	1 +	None	10 1001 1MMM MMMM

	(M) = 0	(skip)		
INCMSZ M, a	(M) + 1 → (acc), skip if (M) = 0	1 + (skip)	None	10 1001 0MMM MMMM
IODIR M	Set i/o direction	1	None	10 0000 0000 0MMM
IORAM M, m	(M) ior (acc) → (M)	1	Z	10 1111 1MMM MMMM
IORAM M, a	(M) ior (acc) → (acc)	1	Z	10 1111 0MMM MMMM
IORLA I	Literal ior (acc) →(acc)	1	Z	11 0011 I I I I I I I I
LCALL I	Call subroutine. However, LCALL can addressing 1K address	2	None	01 0 I I I I I I I I I I I
LGOTO I	Go branch to any address	2	None	01 1 I I I I I I I I I I I
MOVAM m	Move data form acc to memory	1	None	10 0000 1MMM MMMM
MOVLA I	Move literal to accumulator	1	None	11 0001 I I I I I I I I I
MOVM M, m	(M) → (M)	1	Z	10 0011 1MMM MMMM
MOVM M, a	(M) → (acc)	1	Z	10 0011 0MMM MMMM
NOP	No operation	1	None	10 0000 0000 0000
RET	Return	2	None	11 1111 0111 1111
RETI	Return and enable INTM	2	None	11 1111 1111 1111
RETLA I	Return and move literal to accumulator	2	None	11 1100 I I I I I I I I
RLM M, m	Rotate left from m to itself	1	C	10 1100 1MMM MMMM
RLM M, a	Rotate left from m to acc	1	C	10 1100 0MMM MMMM
RRM M, m	Rotate right from m to itself	1	C	10 1110 1MMM MMMM
RRM M, a	Rotate right from m to acc	1	C	10 1110 0MMM MMMM
SELECT	Set select register	1	None	10 0000 0000 0010
SLEEP	Enter sleep (saving) mode	1	$\overline{TO}$, $\overline{PD}$	10 0000 0000 0011
SUBAM M, m	(M)–(acc) → (M)	1	C, DC, Z	10 1010 1MMM MMMM
SUBAM M, a	(M) –(acc) → (acc)	1	C, DC, Z	10 1010 0MMM MMMM

SWAPM M, m	Swap data from m to itself	1	None	10 1101 1MMM MMMM
SWAPM M, a	Swap data from m to acc	1	None	10 1101 0MMM MMMM
XORAM M, m	(M) xor (acc) → (M)	1	Z	10 1011 1MMM MMMM
XORAM M, a	(M) xor (acc) → (acc)	1	Z	10 1011 0MMM MMMM
XORLA I	Literal xor (acc) → (acc)	1	Z	11 1000 I I I I I I I I

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V Storge Temperature ……. –50°C to 125°C

Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature …. 0°C to 70°C

9.2 DC Characteristics

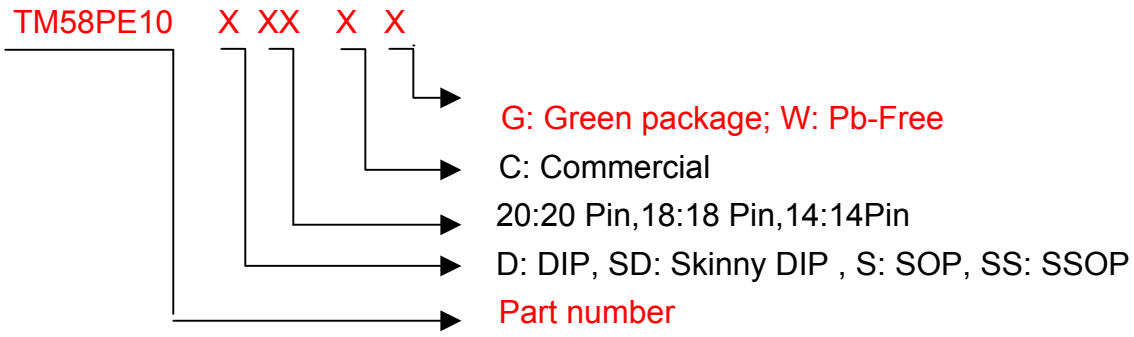
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		2.2		5.5	V
V_{DVT}	Detect Voltage	5V	Low Voltage Detector (Idd = 3uA) Config bit6.bit5=00		4		V
		3V	Low Voltage Detector (Idd = 1.5uA) Config bit6.bit5=10		2.3		V
V_{IH}	Input High Voltage	5V	I/O Port	2		VDD	V
V_{IL}	Input Low Voltage	5V	I/O Port			0.8	V
I_{DD1}	Standby Current	5V	LVD disable, WDT disable		1		uA
			LVD disable, WDT enable		10		
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS		1		uA
I_{OH}	I/O Port Driving Current	5V	Voh=4.5V		9		mA
			Voh=4V		17		
			Voh=3.5V		23		
		3V	Voh=2.5V		6.5		
			Voh=2V		10		
I_{OL}	I/O Port Sink Current	5V	Vol=0.5V		20		mA
			Vol=01V		35		
			Vol=1.5V		50		
		3V	Vol=0.5V		10		
			Vol=01V		20		
			Vol=1.5V		25		
R_{PUHI}	Pull_Hi Pin Resister	5V	Set PortB input pin and Pull_Hi		60		KΩ
		3V	Set PortB input pin and Pull_Hi		150		

9.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
		VDD	Conditions				
f_{sys1}	System Clock	5V 3V	LP Crystal mode	32 32		200 200	Khz
f_{sys2}	System Clock	5V 3V	NT Crystal mode	0.2 0.2		10 10	Mhz
f_{sys3}	System Clock	5V 3V	HS Crystal mode	10		20	Mhz
f_{sys4}	System Clock	5V 3V	RC mode			10 10	Mhz
T_{wdt}	Watchdog Timer	5V 3V	(Default value)		16 20		mS
T_{rht}	Reset Hold Time	5V 3V	(Default value)		16 20		mS

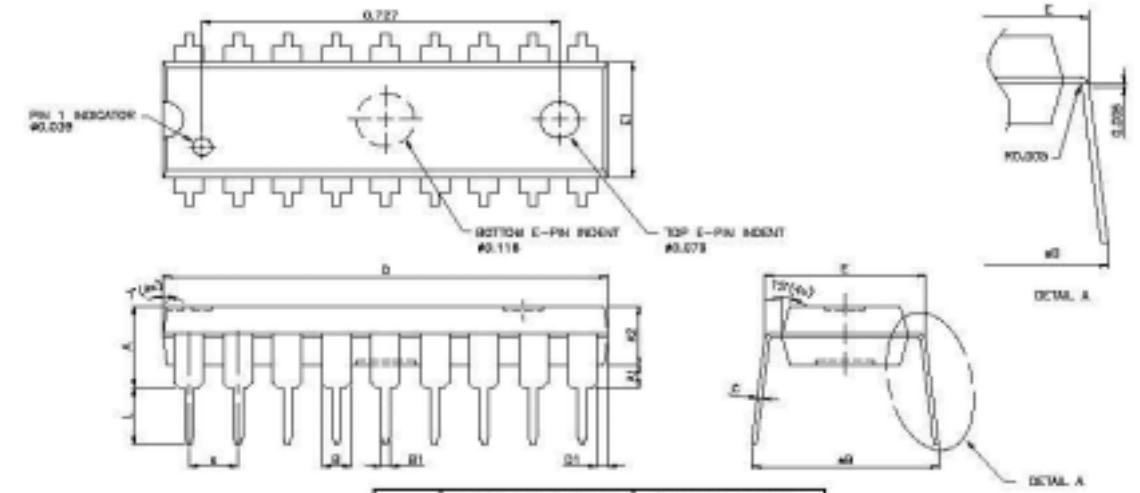
9.4 Packaging Diagrams and Description

9.4.1 Part number Guide



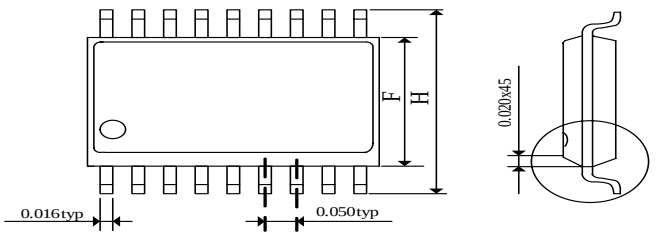
9.4.2 Package mode

(1) 18Pin DIP (300 mil)



P-DIP 18PIN-300MIL

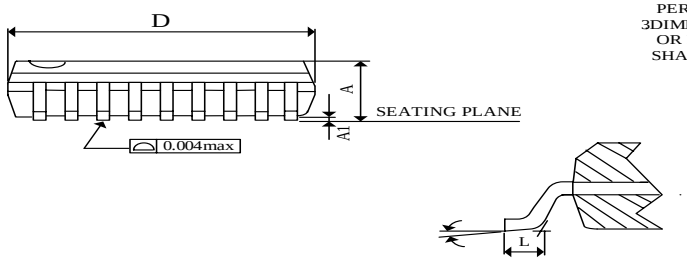
(2) 18Pin SOP (300 mil)



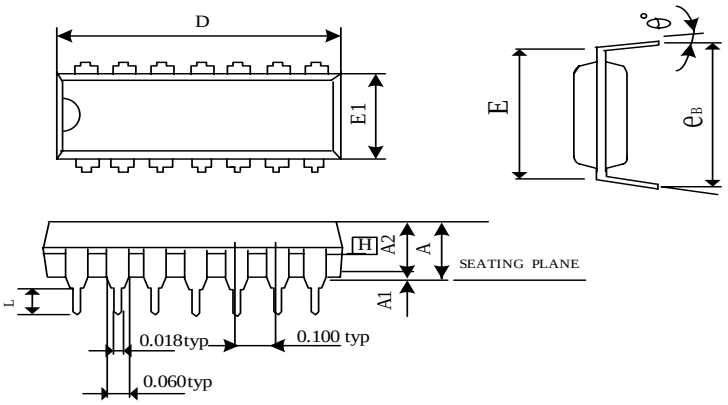
Symbol	MIN	MAX
A	0.093	0.104
A1	0.004	0.012
D	0.447	0.463
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT:INCH

Note:
1. JEDEC OUTLINE: MS-013 AB
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (.006in) PER SIDE
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (.010in) PER SIDE.



(3) 14Pin DIP (300 mil)



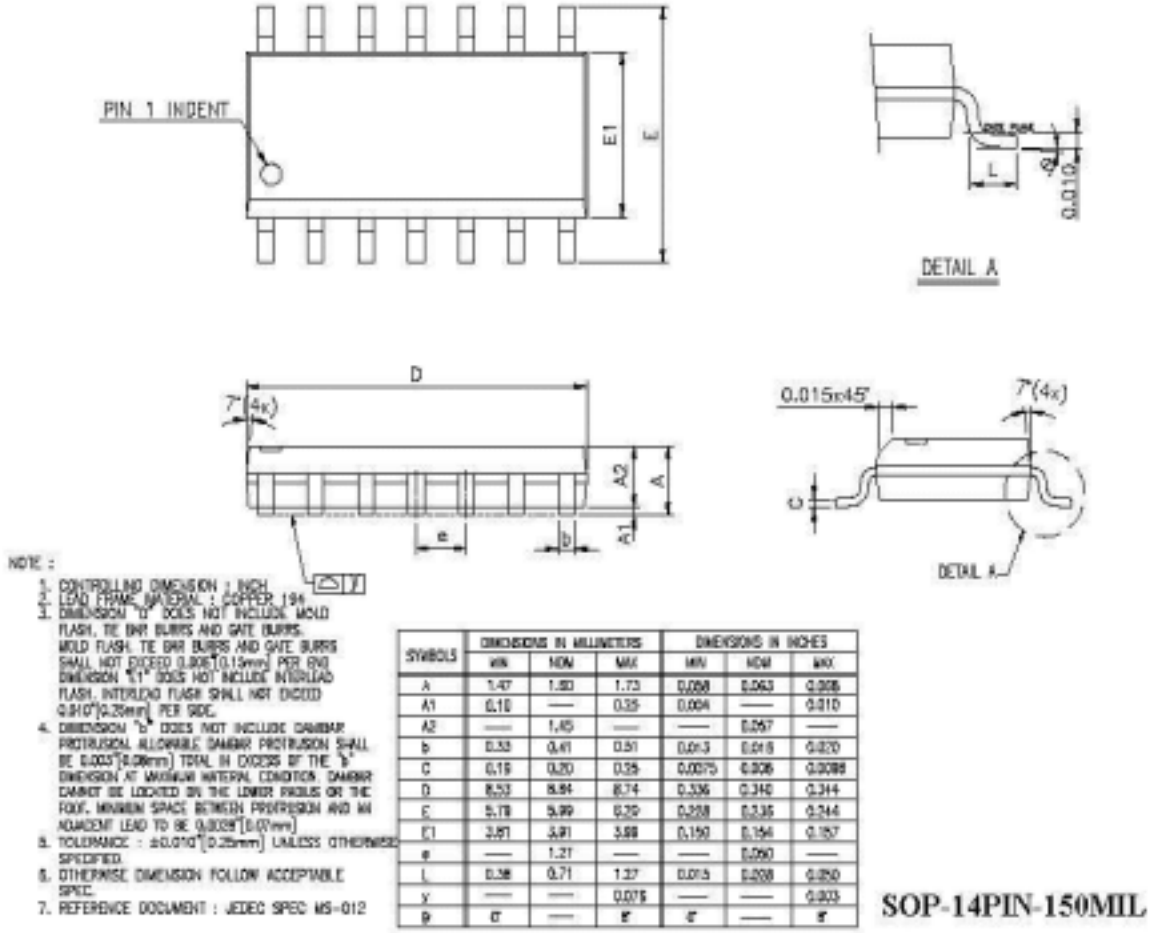
SYMBOLS	MIN	NOR	MAX
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1.JEDEC OUTLINEMS-001 AA

3.eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED
4.POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION
5.DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINNUM
6.DATUM PLANE H COINCIDENT WITH THE BOTTON OF LEAD,WHERE LEAD EXITS BODY.

(4) 14Pin SOP (150 mil)

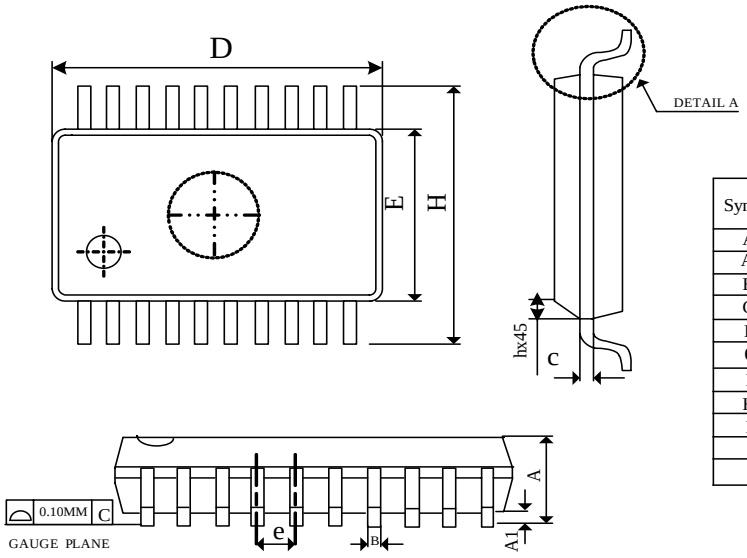


NOTE :
1. CONTROLLING DIMENSION : INCH.
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.007"[0.07mm].
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	8.53	8.64	8.74	0.336	0.340	0.344
E	5.79	5.99	6.20	0.228	0.235	0.244
E1	3.81	3.91	3.98	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

SOP-14PIN-150MIL

(5) 20 Pin SSOP (209 mil)



Symbol	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.0091	0.0125
D	12.60	13.00	0.4961	0.5118
e	1.27 BSC		0.050 BSC	
E	7.40	7.60	0.2914	0.2992
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

*Note: DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.