1. Feature

ROM: 1K x 14 bits (Mask ROM)

RAM: 24 x 8 bits

STACK: 4 Levels

I/O ports: 18-pin (PA7 ~ PA0, PB5 ~ PB0, PC2 ~ PC0, REM)

Timer/counter: 8bits x1 (TMR0)

Prescaler: 3 bits

Reset : 1. Power-On Reset
2. Low voltage reset
3. Wake-up(Release from sleep mode)

Oscillate : NT mode

Operation Voltage: 1.8V～3.6V

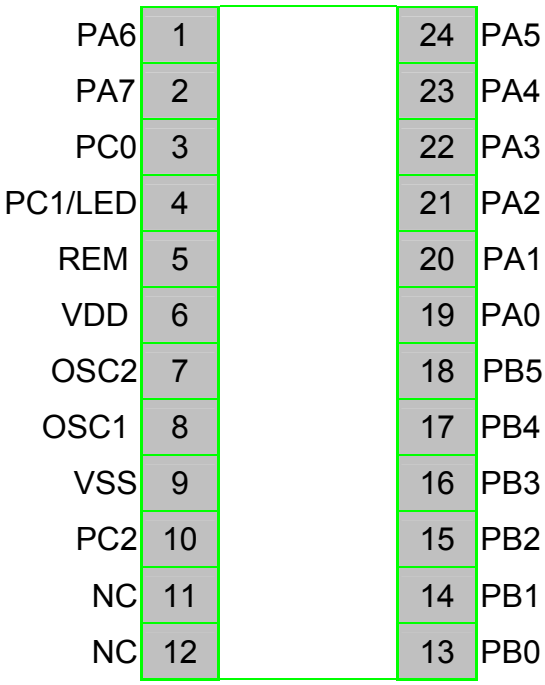
Instruction set: 75

Wake-up: PB5 ~ PB0, PC2 ~ PC0 .

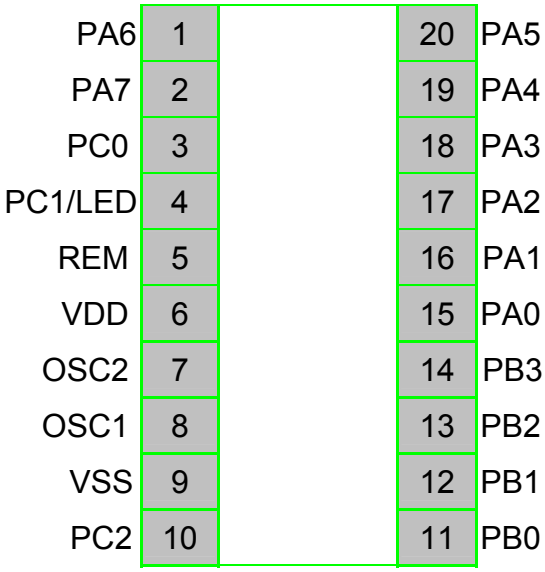
IRQ vector: 3FEH

Reset vector: 3FFH

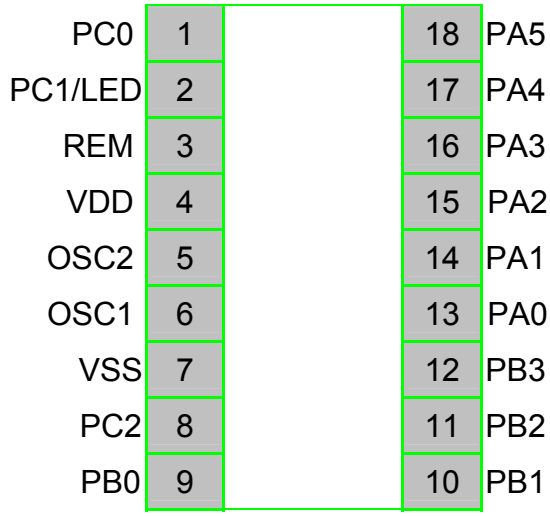
2. Pin Definition & Pad Assignment



Package Types : SOP (TM58RR10S24C)
SSOP(TM58RR10SS24C)



Package Types : SOP (TM58RR10S20C)
SSOP (TM58RR10SS20C)



Package Types : SOP (TM58RR10S18C)
SDIP(TM58RR10SD18C)

3. PIN description

Pin name	I/O	Description
PA(7-0)	I/O	Bi-directional 8-bit input/output port with input pull-down resistors.
PB(5-0)	I	The PB port is a 6-bit input port with pull-down resistors.
PC0	I	The PC0 port is an input/OFF mode port with pull-down resistor.
PC1	I/O	The PC1 port is an I/O port with pull-down resistor.
PC2	I	The PC2 port is an input port with pull-down resistor.
REM	O	Carrier output pin(Remote control output).
OSC1	I	Oscillator input
OSC2	O	Oscillator output
VDD	P	Power input
VSS	P	Ground input

I: Input; O: Output; I/O: Bi-direction; P: Power

4. Control Register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG								LV	CPT
IAR	$00				A4	A3	A2	A1	A0
TMR0	$01	D7	D6	D5	D4	D3	D2	D1	D0
PC	$02	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	$03					$\overline{PD}$	Z	DC	C
BSR	$04				D4	D3	D2	D1	D0
PortA	$05	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PortB	$06			PB5	PB4	PB3	PB2	PB1	PB0
PortC	$07						PC2	PC1	PC0
MODL	$20	ML7	ML6	ML5	ML4	ML3	ML2	ML1	ML0
MODH	$21	MH7	MH6	MH5	MH4	MH3	MH2	MH1	MH0
IRQ	$22	INTM							INTF
PGS	$23							PGS1	PGS0
PSTAT	$24	PB Wake-up	PC Wake-up	PB Pull-down	PC1/ PC0 Pull-down	PC2 Pull-down	PC1 mode		PC0 mode
CG_CTL	$25					REM	LEVEL	MH8	ML8
TMR0_CTL	$26				Load	TMR0EN	PS2	PS1	PS0

4.1 IAR and BSR Register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BSR	$04	+	+	+	D4	D3	D2	D1	D0
Value (After cold reset)		1	1	1	X	X	X	X	X

※ X: unknown, +:unimplemented and read as"1".

The IAR (indirect addressing register) is not a physical register. The BSR (bank select register) is associated with IAR to indirectly access the data memory Any instruction attempts to access IAR actually mapping to another address that is pointed by BSR. Since IAR is not a material circuit. that user reads IAR itself (when BSR=00H) will always return 00h at data bus. Writing to IAR itself (when BSR=00H) will be like a NOP instruction. BSR is a 5-bit wide register which Only can point to the data memory address 00h~1Fh. User can't access out of the range by using IAR register. The addressing map is shown in Figure 4-1.

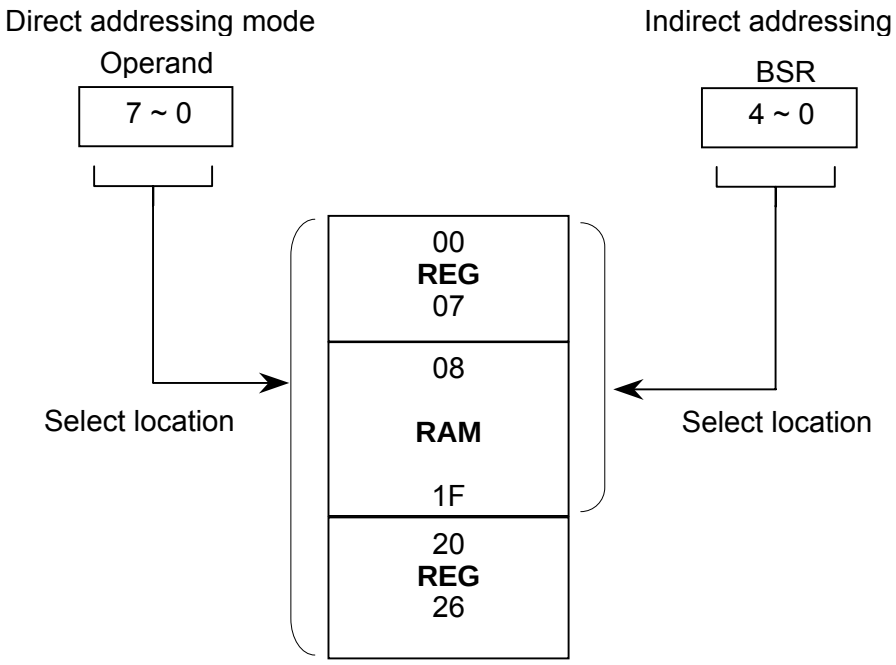


Figure 4-1 The Direct and Indirect Addressing Map

4.2 TMR0 and TMR0_CTL Register

TMR0 register and pre-load TMR0 (see Figure 4-3) are 8-bit wide binary counter. This register decreases by internal instruction cycle. It has the following features.

A. Readable and writeable.

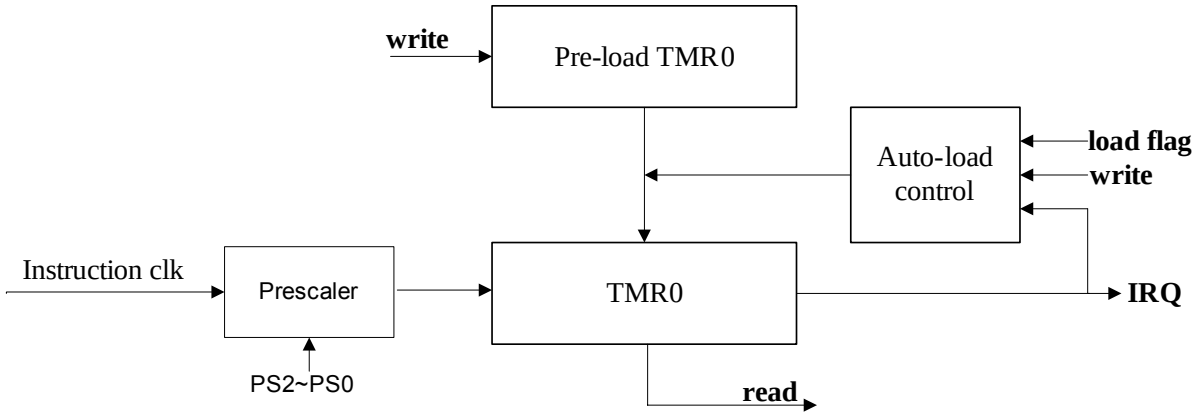
B. Can use programmable prescaler by setting TMR0_CTL(show in Figure 4-2)register.

C. System will generate a interrupt request when TMR0 count down to zero.

Control register TMR0_CTL (26H)				
Bit	Symbol	reset	Description	
4	Load	1	TMR0 data load mode 1: If any operating instruction write data to TMR0 data register, The context of TMR0 will be modified immediately. 0: If any operating instruction write data to TMR0 data register, The context of TMR0 won't be modified immediately until Timercounter overflow.	
3	TMR0EN		TMR0 enable flag 1: Start counting 0: Stop counting	
2~0	PS2~PS0		PS2~ PS0	TMR0 RATE
			000	1 : 1
			001	1 : 2
			010	1 : 4
			011	1 : 8
			100	1 : 16
			101	1 : 32
			110	1 : 64
			111	1 : 128

Figure 4-2 The TMR0_CTL register

Fig. 4-3 shows the block diagram of the TMR0 register, pre-load TMR0 and Prescaler. As shown in the figure, the prescaler register can be a pre-divider for TMR0.



Instruction / Counter	Write 01H	Read 01H
Pre-load TMR0	V	X
TMR0	Decided by Load flag of TMR0_CTL	V

※ Reading from address 01H will push TMR0 value to Accumulator

※ Writing to address 26H will push Accumulator value to Pre-load TMR0.
If Load flag of TMR0_CTL has be set to 1,the context of TMR0 will be modified immediately.

Figure 4-3 Block diagram of the TMR0 and Prescaler

4.3 PC Register

PC (program counter) is 10-bit wide binary counter and increases itself for every instruction cycle, except the following conditions.

1. lgoto and lcall: the label will move to PC
2. retla ,ret and reti: the top level of stack will pop to PC

Incrementing PC when it changes to the next page. It should be noted that the page select bits in the PGS register would not be changed synchronously. The instruction MOVAM 02H will return to the previous page, unless the page select bits have been updated in program. In order to reduce the complexity of programming. LCALL and LGOTO have 10-bit wide operands that are easy to address the total ROM space.

4.4 STATUS Register

Status register contains power down bit and the status of ALU. Please note that $\overline{PD}$ are controlled by hardware and unchangeable by program.

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">0</td><td rowspan="3">C</td><td colspan="2">Carry and $\overline{Borrow}$ bit:</td></tr>
<tr><td>ADD instruction</td><td>SUB instruction</td></tr>
<tr><td>1:a carry occurred from the MSB
0: no carry</td><td>1: no borrow (Note1)
0:a borrow occurred from the MSB</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">DC</td><td colspan="2">Nibble Carry and Nibble $\overline{Borrow}$ bit</td></tr>
<tr><td>ADD instruction</td><td>SUB instruction</td></tr>
<tr><td>1: a carry from the low nibble bits of the result occurred
0: no carry</td><td>1: no borrow
0: a borrow from the low nibble bits of the result occurred</td></tr>
<tr><td>2</td><td>Z</td><td colspan="2">Zero bit:
1: the result of a logic operation is zero
0: the result of a logic operation is not zero</td></tr>
<tr><td>3</td><td>$\overline{PD}$</td><td colspan="2">Power down flag bit: (Note2)
1: Power on reset
0: Wake-up from sleep</td></tr>
</table>

Figure 4-4 Status Register

Note1: A SUB instruction is executed by adding the 2's complement of the subtrahend, so C = 1 represents positive result. The Figure 4-5 show the relation between C-bit and borrow.

Note2: The $\overline{PD}$ bit can be used to determine different causes of reset.

B0H－50H										**50H－B0H**									
	C	B7	B6	B5	B4	B3	B2	B1	B0		C	B7	B6	B5	B4	B3	B2	B1	B0
＋		1	0	1	1	1	0	0	0	＋		0	1	1	0	1	0	0	0
＝	1	0	1	1	0	0	0	0	0	＝	0	1	0	1	0	0	0	0	0

Figure 4-5

4.5 PortA register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PortA	$05	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
I/O (After cold reset)		IN/R	IN/R	IN/R	IN/R	IN/R	IN/R	IN/R	IN/R
Value (After cold reset)		0	0	0	0	0	0	0	0

※ IN/R represents input mode with a pull-down resistor

※ “cold reset” : please refer to the section 7.1

Port A are programmable I/O ports. The I/O mode is set by instruction “IODIR 05h”. All I/O pins were set to be input mode after reset. In input mode, the pull-down resistor is automatically connected. In output mode, the pull-down resistor is automatically disconnected.

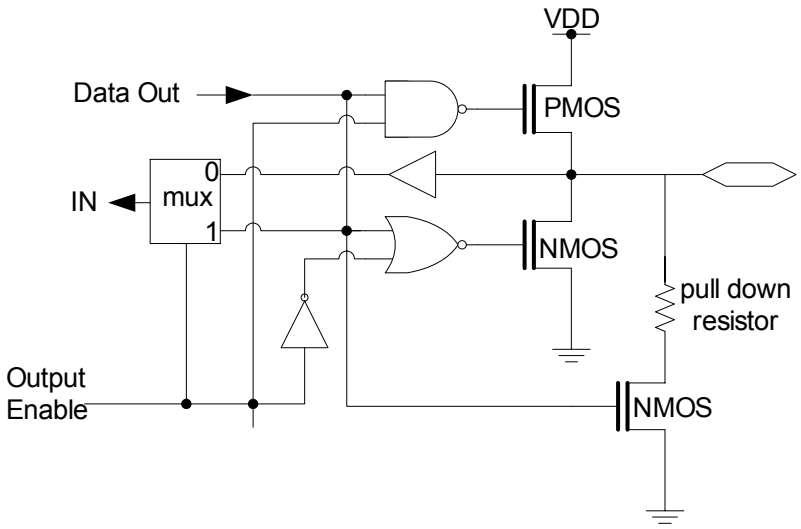


Figure 4-6 Block diagram of the PA port

Example: Set the PA to be output mode and the output value of the PA is 5Ah.

```
MOVLA    00h;
IODIR    05h; set all of the PA pins to be output mode.
MOVLA    5Ah;
MOVAM    05H; set output value of the PA for 5Ah.
```

4.6 PortB register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PortB	$06			PB5	PB4	PB3	PB2	PB1	PB0

The PB port is a 6-bit input port. The pin state can be read by using “MOVM 06h,A” instruction. The pull-down resistors for the PB port can be specified by setting PSTAT[5]. In PB ports and PC ports , we provide wake up function. Chip can be wake up from Sleep mode when the logic of the PortB or the PortC is changed. So we need to read the logic of the input pin before sleep. In PB ports, You can set the bit7 of PSTAT register to enable or disable wakeup function . If the chip wake up from sleep mode, the warm-reset(refer to the section 7.1) will occur. Program Counter may change to address 3FFh.The block diagram of the PB port is shown in Figure 4-7.

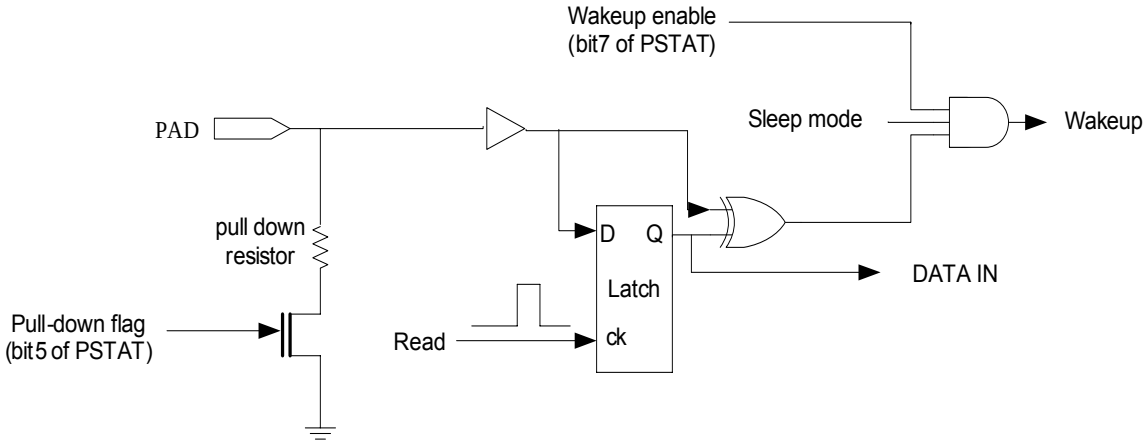


Figure 4-7 Block diagram of the PB port

Example: Wake up from PB ports

```
                ORG     00H ;;
POWERON         BTMSS   03H,b3 ;;
                LGOTO   WAKEUP_IN ;;
                ,,,
                BSM     24h,b7 ;; enable PB wakeup function.
                MOVM    06h,ACC ;; read the logic of the PB pins before sleep.
                SLEEP ;;
                ORG     3FFH ;;
                LGOTO   POWERON ;;
```

4.7 PortC register

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PortC	$07	-	-	-	-	-	PC2	PC1	PC0

※ - unimplemented and read as"0".

4.7.1 PC0

The PC0 port is an input/OFF mode port. In input mode, the pull-down resistors for the PC0 and PC1 ports can be specified by setting PSTAT[4]. If input mode is released (thus set to OFF mode), the pin becomes high-impedance so that through current does not flow internally. In OFF mode, 1 can be read regardless of the pin state. In PB ports and PC ports , we provide wake up function. Chip can be wake up from Sleep mode when the logic of the PortB or the PortC is changed. So we need to read the logic of the input pin before sleep. In PC_0 port, You can set the bit6 of PSTAT register to enable or disable wakeup function . If the chip wake up from sleep mode, the warm-reset(refer to the section 7.1) will occur. Program Counter may change to address 3FFh.The block diagram of the PC_0 port is shown in Figure 4-8.

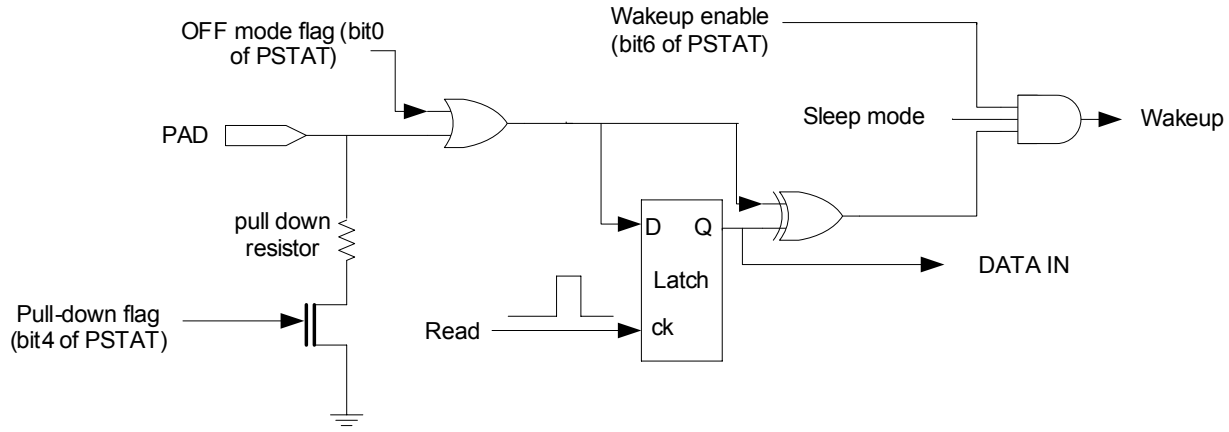


Figure 4-8 Block diagram of the PC0 port

Example: Wake up from PC0 ports

```
                ORG       00H
POWERON         BTMSS     03H,b3 ;;
                LGOTO     WAKEUP_IN ;;
                BSM       24h,b6 ;; enable PC wakeup function.
                MOVM      07h,ACC ;; read the logic of the PC pins before sleep.
                SLEEP ;;
                ORG       3FFH;;
                LGOTO     POWERON
```

4.7.2 PC1

The PC1 port is an I/O port. Input or output mode can be set by using bit 2 of the PSTAT register. The pin state can be read in both input mode and output mode. In input mode, the pull-down resistors for the PC0 and PC1 ports can be specified by setting PSTAT[4]. In output mode, the pull-down resistor is automatically disconnected and this pin becomes the remote control transmission display pin. In PB ports and PC ports , we provide wake up function. Chip can be wake up from Sleep mode when the logic of the PortB or the PortC is changed. So we need to read the logic of the input pin before sleep. In PC_1 port, You can set the bit6 of PSTAT register to enable or disable wakeup function . If the chip wake up from sleep mode, the warm-reset(refer to the section 7.1) will occur. Program Counter may change to address 3FFh.The block diagram of the PC1 port is shown in Figure 4-9.

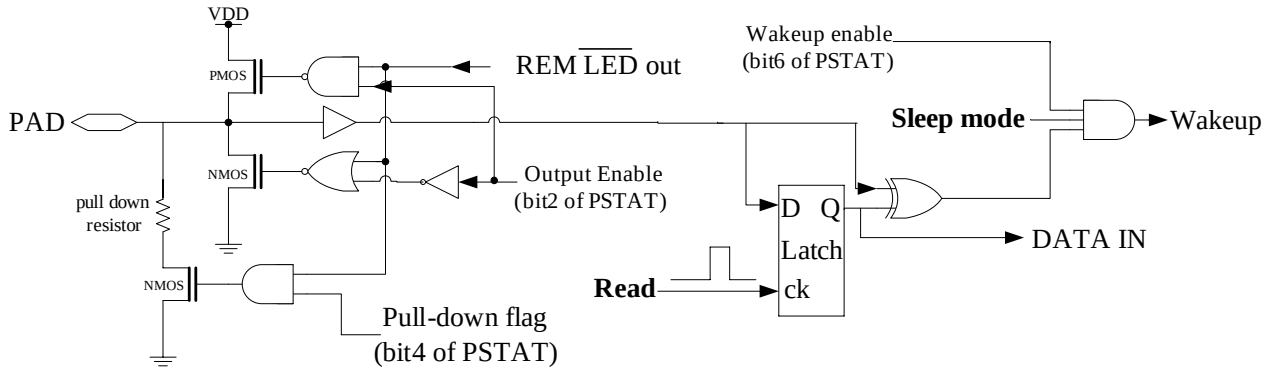


Figure 4-9 Block diagram of the PC1 port

Example: Wake up from PC1 ports

```
                ORG         00H
POWERON         BTMSS       03H,b3 ;;
                LGOTO       WAKEUP_IN ;;
                ,,,
                BSM         24h,b6 ;; enable PC wakeup function.
                BSM         24h,b2 ;; set PC1 to be input mode.
                MOVM        07h,ACC ;; read the logic of the PC pins before sleep.
                SLEEP ;;
                ORG         3FFH ;;
                LGOTO       POWERON ;;
```

4.7.3 PC2

The PC2 port is an input port.

The pull-down resistor for the PC2 port can be specified by setting PSTAT[3]. In PB ports and PC ports , we provide wake up function. Chip can be wake up from Sleep mode when the logic of the PortB or the PortC is changed. So we need to read the logic of the input pin before sleep. In PB ports, You can set the bit6 of PSTAT register to enable or disable wakeup function . If the chip wake up from sleep mode, the warm-reset(refer to the section 7.1) will occur. Program Counter may change to address 3FFh.The block diagram of the PC2 port is shown in Figure 4-10.

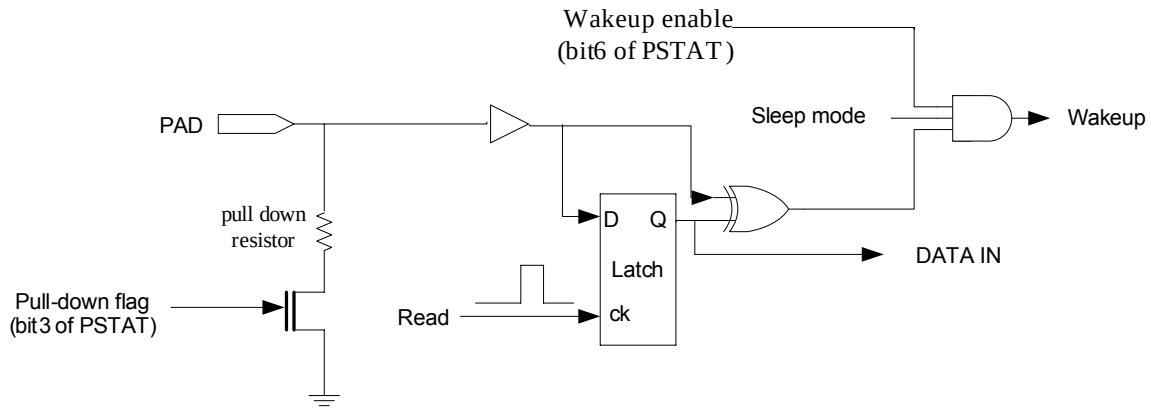


Figure 4-10 Block diagram of the PC2 port

Example: Wake up from PC2 ports

```
                ORG   00H
POWERON         BTMSS       03H,b3 ;;
                LGOTO       WAKEUP_IN ;;
                ,,,
                ,,,
                BSM         24h,b6 ;; enable PC wakeup function.
                MOVM        07h,ACC ;; read the logic of the PC pins before sleep.
                SLEEP ;;
                ORG         3FFH ;;
                LGOTO       POWERON ;;
```

4.8 MODL , MODH and CG_CTL registers

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODL	$20	ML7	ML6	ML5	ML4	ML3	ML2	ML1	ML0
After cold reset		1	1	1	1	1	1	1	1

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MODH	$21	MH7	MH6	MH5	MH4	MH3	MH2	MH1	MH0
After cold reset		1	1	1	1	1	1	1	1

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CG_CTL	$25	-	-	-	-	REM	LEVEL	MH8	ML8
After cold reset		0	0	0	0	0	0	0	0

※ “cold reset” : please refer to the section 7.1

※ -:unimplemented and read as”0”.

The carrier generator consists of a 9-bit counter and two modulo registers for setting the high- and low-level periods (MH8~0 and ML8~0 respectively). The carrier duty ratio and carrier frequency can be determined by setting the high- and low-level widths using the respective modulo registers. Each of these widths can be set in a range of 125ns to 64us (when sysclk = 4 MHz). The system clock multiplied by 2 is used for the 9-bit counter input (8 MHz when sysclk = 4 MHz). See block diagram of the Carrier Generater in figure 4-11.

The values of ML and MH can be calculated from the following expressions.

ML = (2 * sysclk * (1-D) * T)

MH = (2 * sysclk * D * T)

Caution Be sure to input values in range of 001H to 1FFH to ML and MH.

Remark D: Carrier duty ratio (0 < D < 1)

sysclk: System clock (MHz)

T: Carrier cycle (us)

Example: Clock Source = 4MHz, 1/3Duty, Output = 38kHz

Ans: MODL = 2*4M*(1-1/3)*(1/38K) = 8CH→17.50us(standard 17.54us).

MODH=2*4M*(1/3)*(1/38K) = 46H→8.75us(standard 8.77us).

REM = 38.008kHz.

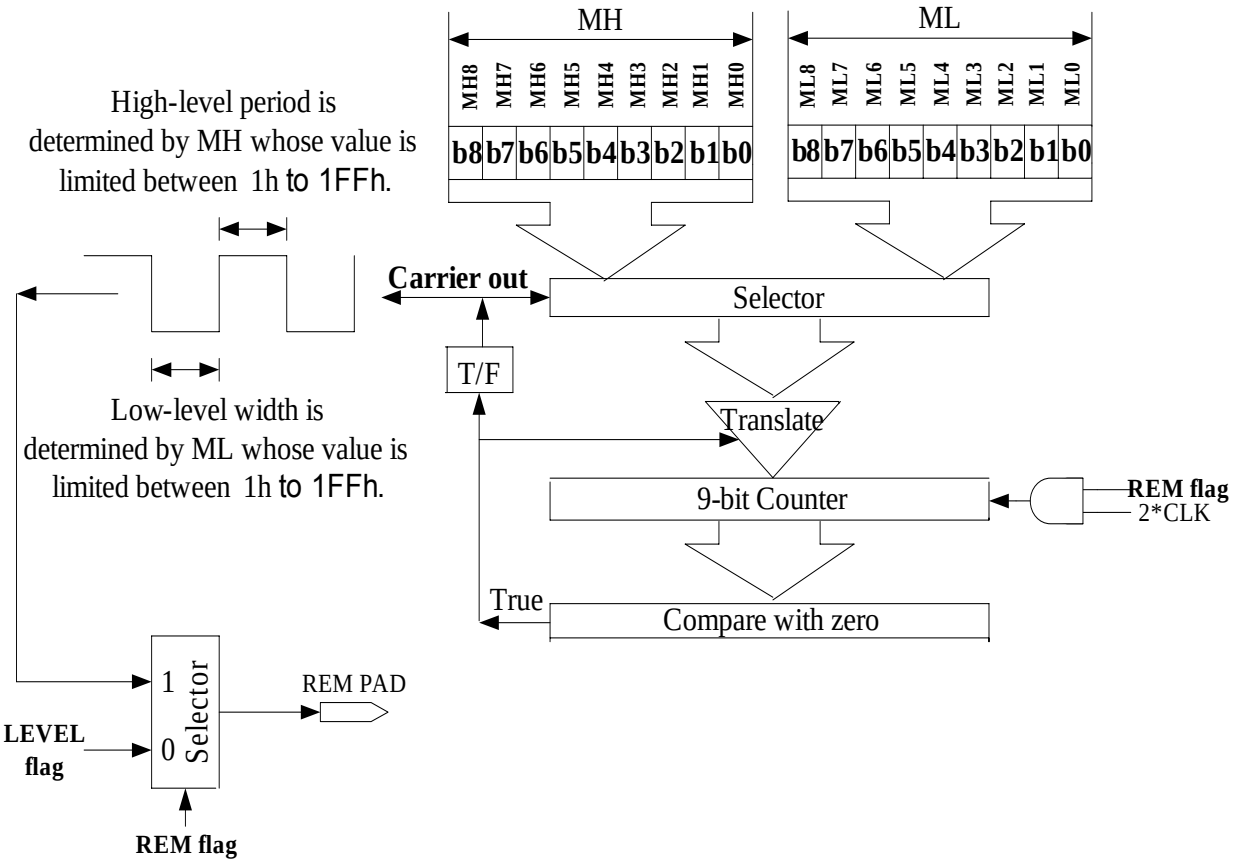


Figure 4-11 Block diagram of the Carrier Generater

4.9 IRQ register

Control register IRQ (22H)			
Bit	Symbol	cold reset	Description
7	INTM	0	Interrupt Mask 1: enable interrupt. 0: disable interrupt.
0	INTF	0	Interrupt Flag 1: The TMR0 counter overflow generates an interrupt request.

※ “cold reset” : please refer to the section 7.1

Program Counter can be transferred by interrupts request. The interrupt performs a transfer by pushing PC onto the top level of stack and then branching to the interrupt vector address (3FEh). The Interrupt Mask flag(INTM) is used to disable or enable the interrupt request.

Note: Interrupt Flags is set by hardware; software can only clear the flag.
It is useless that attempt writing ‘1’ to flag.

4.10 PGS register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGS	$23	-	-	-	-	-	-	PGS1	PGS0
After cold reset		0	0	0	0	0	0	0	0

※ “cold reset” : please refer to the section 7.1

※ -:unimplemented and read as”0”.

System can auto-update PGS register (page select bits) by hardware or write PGS by software. User can use the instructions “LCALL“ and “LGOTO“ they can go anywhere in OTP by hardware. Above-mentioned five instructions take two instruction cycles for operation. See operation diagram in Figure 4-12.

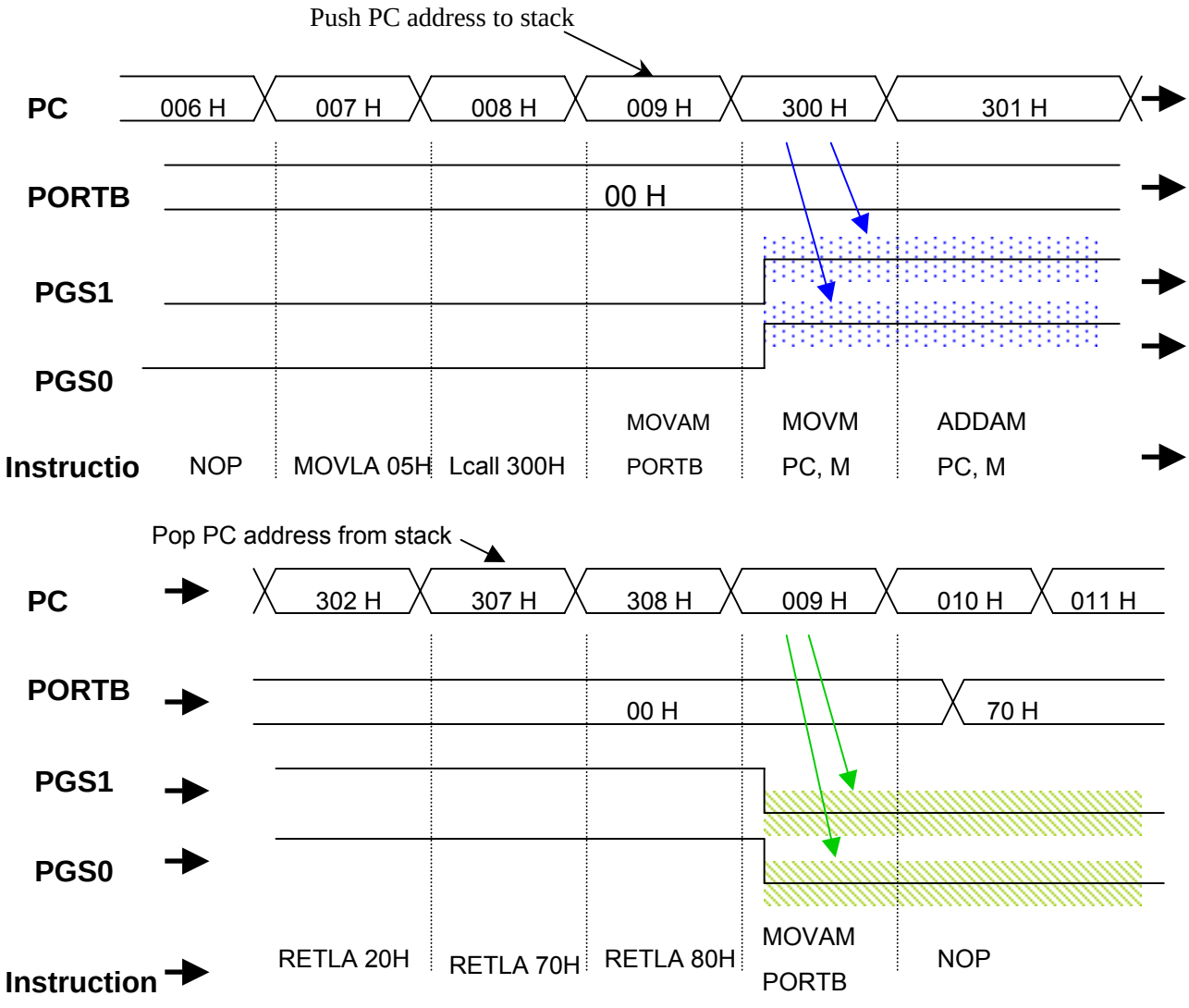


Figure 4-12 PGS[1:0] operation diagram

However user must take a attention when an interrupt has occured. For example, if the PGS register value is 00 and then user set PGS register as 10 by software before interrupt occur. After interrupt occurs, system address to interrupt vector 3FEH. It will auto-update the page select register PGS =11 (page3) by hardware. After interrupt finished, system pop the top level context of stack to Program Counter and set the PGS[1:0] register as 00. Before interrupt occur, PGS register is written =10 will lose. User need to take care of interrupt when you write PGS (page select bits) by yourself. See operation diagram in Figure 4-13.

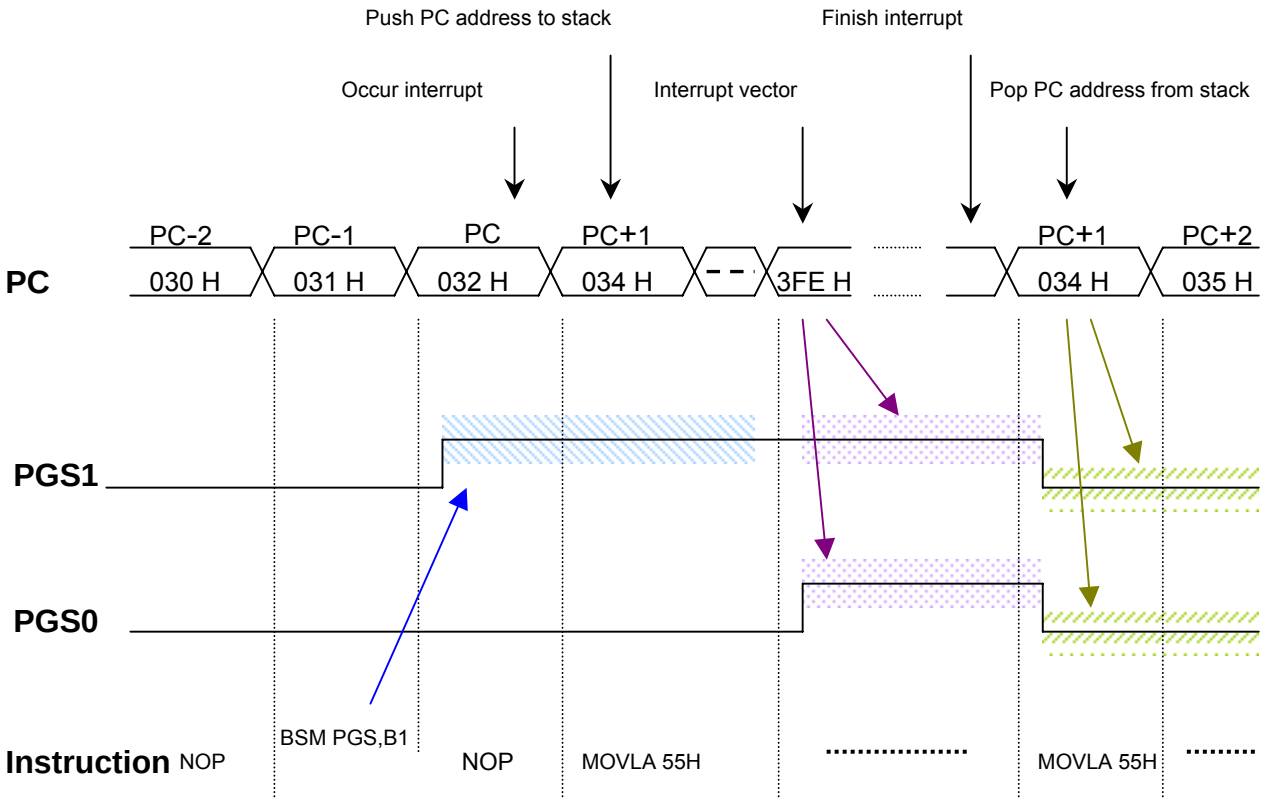


Figure 4-13 PGS [1:0] operation on interrupt diagram

4.11 PSTAT Register

Name		Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSTAT		$24	PB Wake-up	PC Wake-up	PB Pull-down	PC1/ PC0 Pull-down	PC2 Pull-down	PC1 mode	X	PC0 mode
Setting	0		OFF	OFF	OFF	OFF	Disable	$\overline{LED}$	0	OFF
	1		ON	ON	ON	ON	Enable	PC1	0	IN
After cold reset			0	0	1	0	0	0	0	0

※ “cold reset” : please refer to the section 7.1

b0: Specifies the input mode of the PC_0 port.

0 = OFF (high impedance); 1 = IN (input mode).

b1: Reserved;

b2: Specifies the I/O mode of the PC 1/$\overline{LED}$ port.

0 = LED (output mode).; 1 = PC 1 (input mode)

b3: Specifies the use of a pull-down resistor in PC 2.

0 = disable (without pull-down); 1 = enable (with pull-down).

b4: Specifies the use of a pull-down resistor in PC1/ PC0 port input mode.

0 = OFF (not used); 1 = ON (used).

b5: Specifies the use of a pull-down resistor for the PB port.

0 = OFF (not used); 1 = ON (used).

b6: Specifies the wake-up function of PC port.

0 = OFF; 1 = ON.

Chip can be wakeup by changing the state the PC port which be set as input mode.

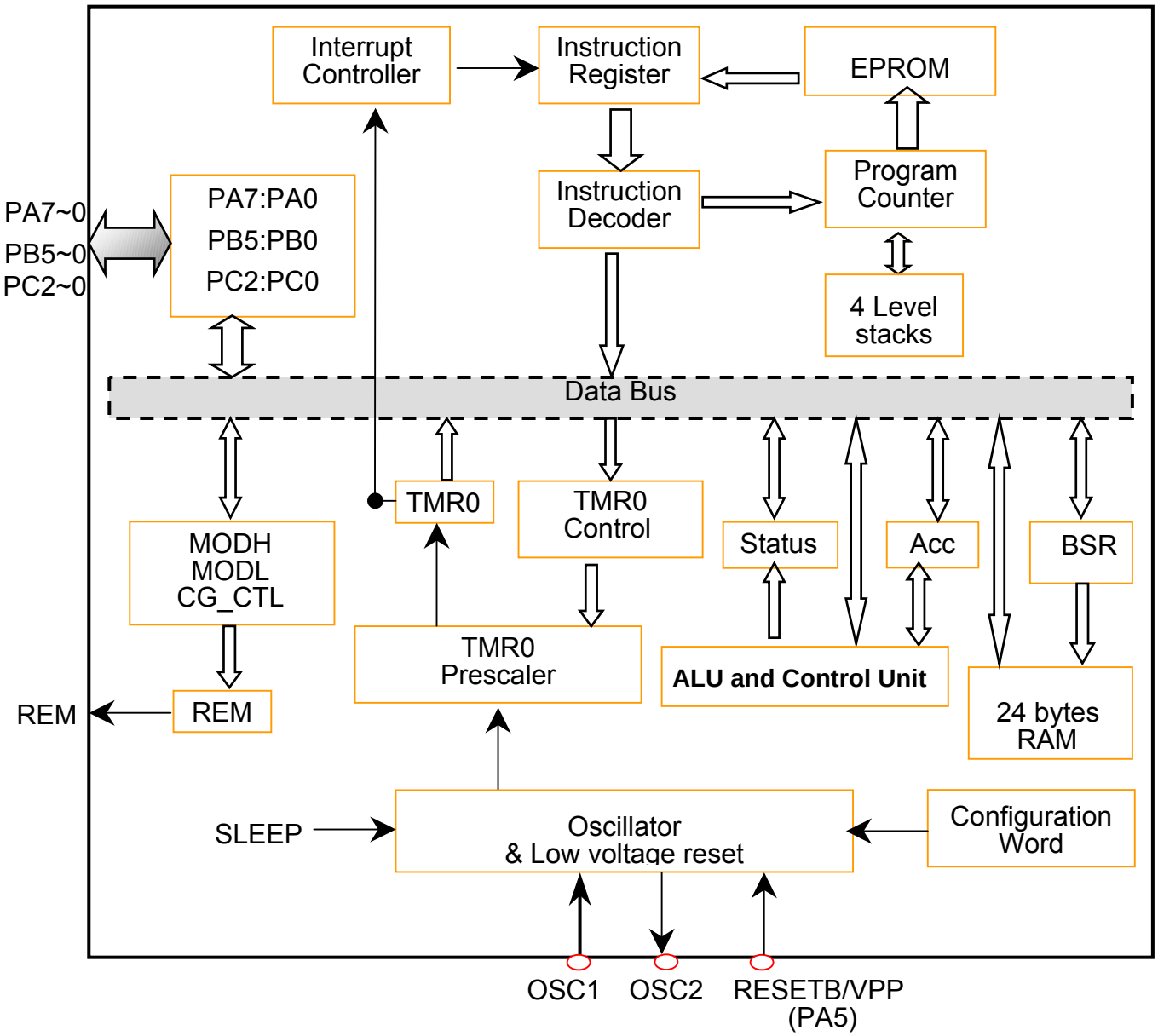
b7: Specifies the wake-up function of PB port.

0 = OFF; 1 = ON.

Chip can be wakeup by changing the state the PB port.

Remark In output mode or in OFF mode, all the pull-down resistors are automatically disconnected.

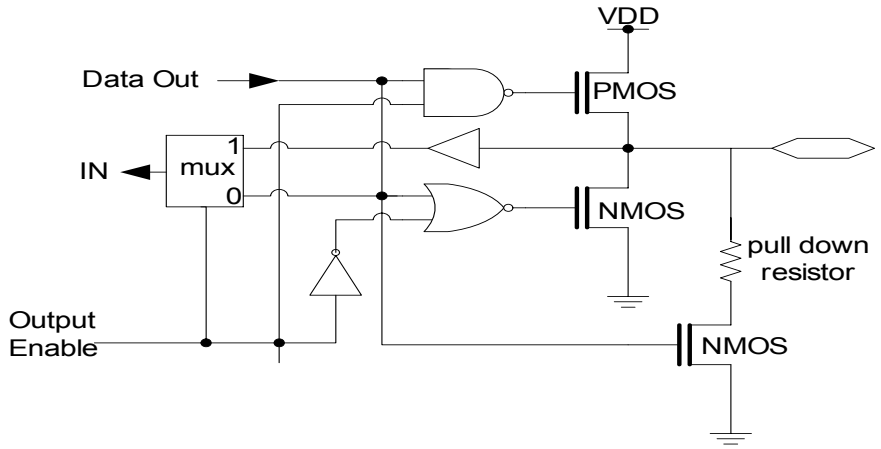
5. SYSTEM BLOCK DIAGRAM



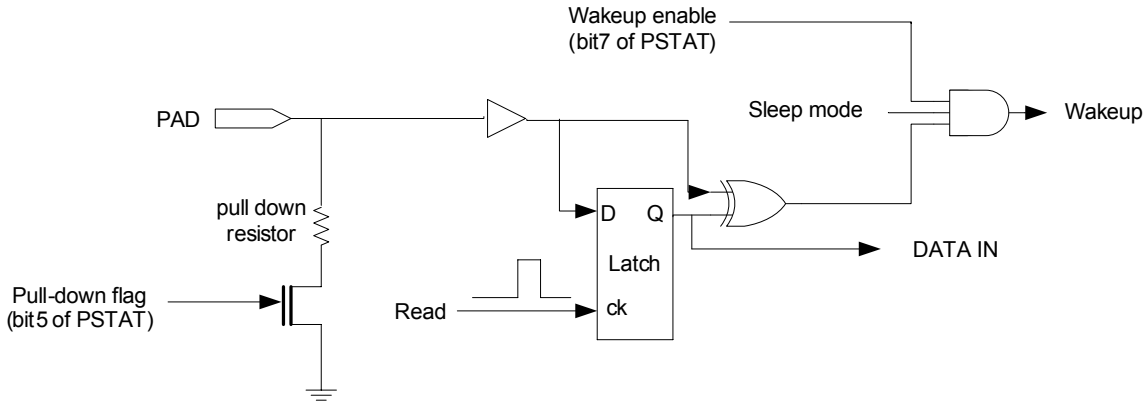
5.1 Pin I/O Circuits

The I/O circuits are shown in partially simplified forms below.

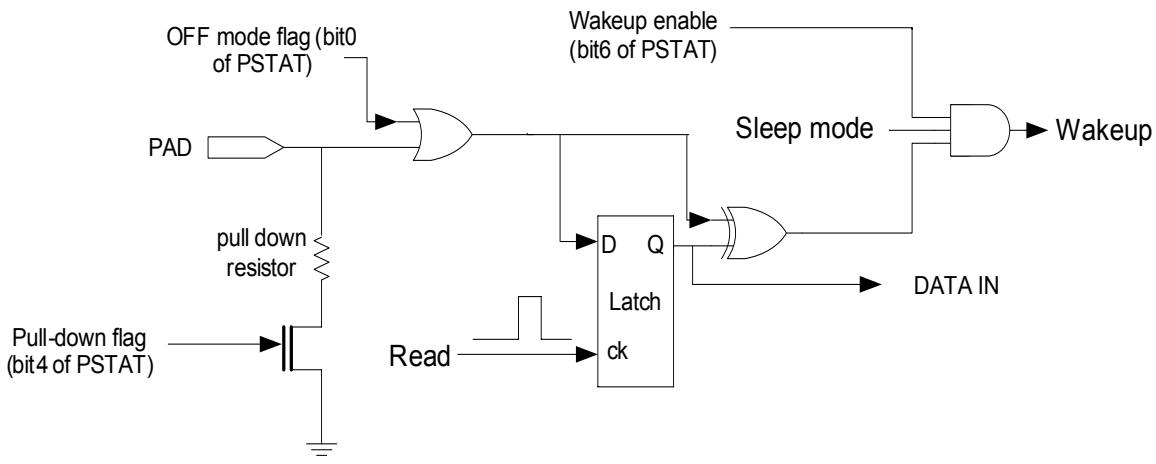
1. PA7 to PA0 (I/O)



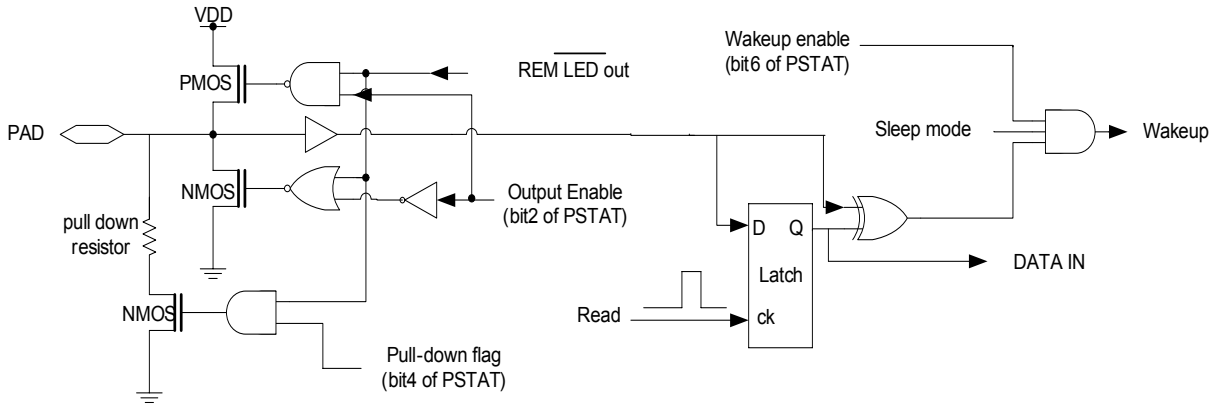
2. PB5 to PB0 (I)



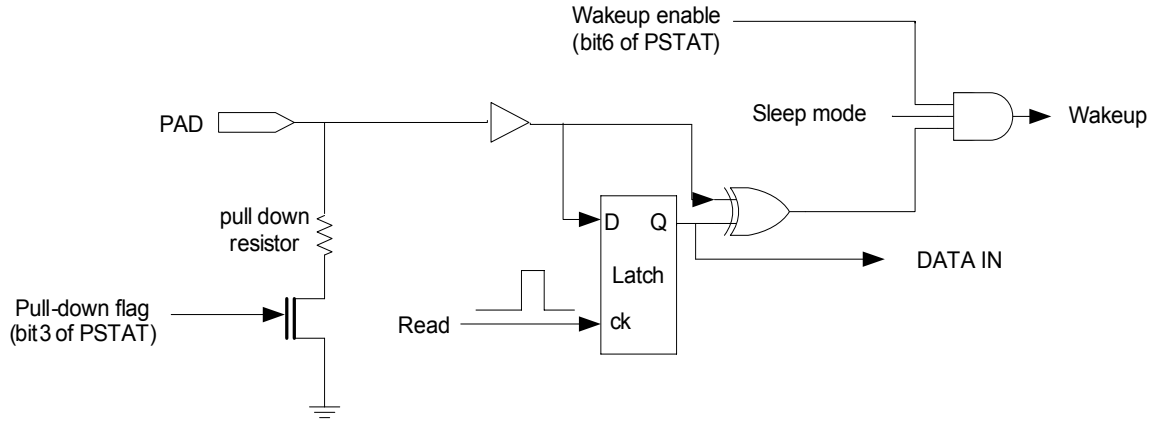
3. PC0 (I)



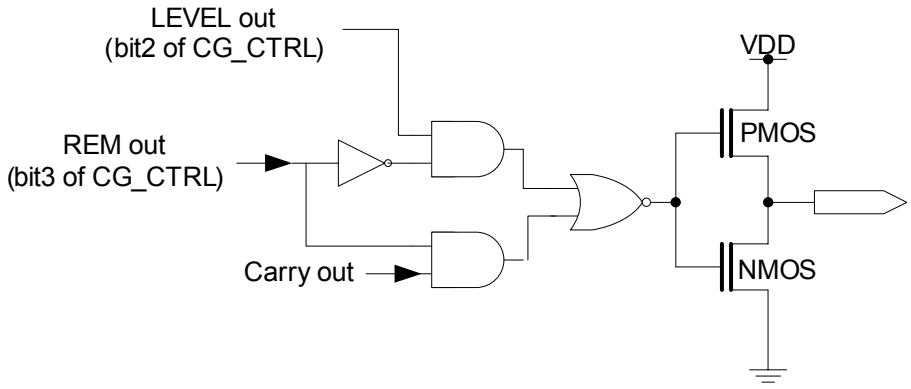
4. PC1 (I/O)



5. PC2 (I)



5. REM (O)



6. Memory Map

TM58RR10 memory is organized into program memory and data memory.

6.1 Program memory

There are only 256 words of the same page that can be directly addressed by using PC register. Extra program memory can be addressed by setting bit 1~0 of PGS register. The sequence of instructions is controlled via the program counter (PC), which automatically increases 1. However, the sequence can be changed by skip, lcall and lgoto instructions or by moving data to the PC.

TM58RR10 has a 10-bits program counter capable of accessing 1K spaces. If accessing address has over 1K, then the address will map to physical 1K memories, i.e. 1K+M will be mapped to M. A simple map to induce illustrate ROM organization is shown in figures 6-1.

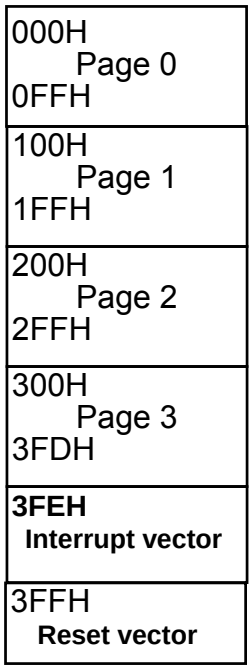


Figure 6-1 The ROM Organization

6.2 CONFIG word (Code option)

The configuration word is located 800H that contains low voltage detecting and code protection selection. The configuration word is shown in figure 6-2

Bit	Symbol	Description	
2	LV	LV	Low Voltage reset
		1	Don't use
		0	System reset when operating voltage is under 2.3V
1	CPT	CPT: Code Protection bit 1: OFF 0: ON	

Figure 6-2 The Configuration Word

6.3 Data memory

Data memory is composed of special function registers and general-purpose ram. TM58RR10 has 24 general-purpose registers that accessed by using a bank select scheme. The special function registers include the program counter (PC), the timer (TMR0) register, the status register, the bank select register, and the I/O port registers. Furthermore, TM58RR10 has 2 auxiliary registers that include indirect addressing register (IAR) and the I/O direction register (IODIR). The register map of general mode is shown in figure 6-3.

00H	IAR
01H	TMR0
02H	PC
03H	STATUS
04H	BSR
05H	PORTA
06H	PORTB
07H	PORTC
08H – 1FH	24 General Purpose Register
20H	MODL
21H	MODH
22H	IRQ
23H	PGS
24H	PSTAT
25H	CG_CTL
26H	TMR0_CTL

Figure 6-3 The Register Map

7. Function Description

7.1 Reset

TM58RR10 may be reset by one of the following conditions:

(1) Power-on.

This event will set the $\overline{PD}$ flag in STATUS register to “1”.

(2) Power-down (circuit protection). refer to electrical characteristic.

This event will set the $\overline{PD}$ flag in STATUS register to “1”.

(3) Wake-up.

This event will set the $\overline{PD}$ flag in STATUS register to “0”.

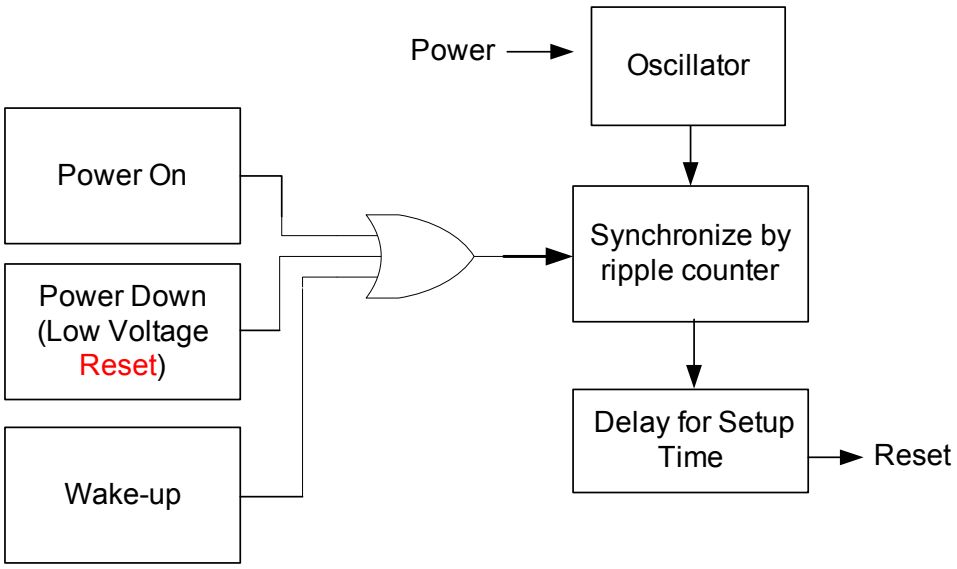


Figure 7-1 Scheme of the Reset Controller

As shown in the figure 7-1, three reset conditions are listed. The power-down event will cause TM58RR10 to reset which the voltage ranges is according to the bit2~bit1 in the configuration word. This condition is used to protect chip in deficient power environment. The voltage ranges of power-down are defined in electrical characteristics. Furthermore, the ranges may be influenced by process and temperature variations. In general, we call the first two reset-cases as cold reset.

The last cases are called warm reset. The different reset events will affect registers and ram. The $\overline{PD}$ bits can be used to determine the type of reset. These relation are listed in figure 7-2

Address	Name	Cold Reset	Warm Reset
N/A	Accumulator	xxxx xxxx	pppp pppp
N/A	IODIR	1111 1111	pppp pppp
00H	IAR	---- ----	pppp pppp
01H	TMR0	xxxx xxxx	pppp pppp
02H	PC	11 1111 1111	11 1111 1111
03H	STATUS	---- 1xxx	---- 0ppp
04H	BSR	+++x xxxx	+++p pppp
05H	PORTA	0000 0000	pppp pppp
06H	PORTB	xxxx xxxx	xxpp pppp
07H	PORTC	---- -xxx	---- -ppp
08H – 1FH	24 General Purpose Register	xxxx xxxx	pppp pppp
20H	MODL	1111 1111	pppp pppp
21H	MODH	1111 1111	pppp pppp
22H	IRQ	0--- ---0	p--- ---p
23H	PGS	---- --00	---- --00
24H	PSTAT	0010 00-0	pppp pp-p
25H	CG_CTL	---- 0000	---- pppp
26H	TMR0_CTL	---0 0000	---p pppp

Figure 7-2 RESET CONDITIONS

X: unknown; P: previous data ; ?: value depends on condition ;
-:unimplemented and read as"0". +:unimplemented and read as"1".

7.2 Sleep and Wake-up

The TM58RR10 will be in the sleep mode after a SLEEP instruction executed. In this mode, the system clock is turned off and the I/O ports and registers retain their status. Thus keep the device consumes less power. The device will wake-up from SLEEP through one of the PB and the PC pins logic in input mode has be changed. Wake-up from SLEEP will produce 1024 system clk delay in any oscillator mode. The wake up reset vector is 3FFh.

8. Instruction Set

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	OP-code
ADDAM M, m	(M)+(acc) → (M)	1	C, DC, Z	10 0101 1MMM MMMM
ADDAM M, a	(M)+(acc) → (acc)	1	C, DC, Z	10 0101 0MMM MMMM
ANDAM M, m	(M) · (acc) → (M)	1	Z	10 0100 1MMM MMMM
ANDAM M, a	(M) · (acc) → (acc)	1	Z	10 0100 0MMM MMMM
ANDLA I	Literal · (acc) (acc)	1	Z	11 1001 iiii iiii
BCM M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BCM M, b1	Clear bit1 of (M)	1	None	00 1100 1MMM MMMM
BCM M, b2	Clear bit2 of (M)	1	None	00 1101 0MMM MMMM
BCM M, b3	Clear bit3 of (M)	1	None	00 1101 1MMM MMMM
BCM M, b4	Clear bit4 of (M)	1	None	00 1110 0MMM MMMM
BCM M, b5	Clear bit5 of (M)	1	None	00 1110 1MMM MMMM
BCM M, b6	Clear bit6 of (M)	1	None	00 1111 0MMM MMMM
BCM M, b7	Clear bit7 of (M)	1	None	00 1111 1MMM MMMM
BSM M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BSM M, b1	Set bit1 of (M)	1	None	00 1000 1MMM MMMM
BSM M, b2	Set bit2 of (M)	1	None	00 1001 0MMM MMMM
BSM M, b3	Set bit3 of (M)	1	None	00 1001 1MMM MMMM
BSM M, b4	Set bit4 of (M)	1	None	00 1010 0MMM MMMM
BSM M, b5	Set bit5 of (M)	1	None	00 1010 1MMM MMMM
BSM M, b6	Set bit6 of (M)	1	None	00 1011 0MMM MMMM
BSM M, b7	Set bit7 of (M)	1	None	00 1011 1MMM MMMM
BTMSC M, b0	If bit0 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTMSC M, b1	If bit1 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 1MMM MMMM
BTMSC M, b2	If bit2 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 0MMM MMMM
BTMSC M, b3	If bit3 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 1MMM MMMM
BTMSC M, b4	If bit4 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 0MMM MMMM
BTMSC M, b5	If bit5 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 1MMM MMMM
BTMSC M, b6	If bit6 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 0MMM MMMM
BTMSC M, b7	If bit7 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 1MMM MMMM

BTMSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTMSS M, b1	If bit1 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 1MMM MMMM
BTMSS M, b2	If bit2 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 0MMM MMMM
BTMSS M, b3	If bit3 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 1MMM MMMM
BTMSS M, b4	If bit4 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 0MMM MMMM
BTMSS M, b5	If bit5 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 1MMM MMMM
BTMSS M, b6	If bit6 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 0MMM MMMM
BTMSS M, b7	If bit7 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 1MMM MMMM
CLRA	Clear accumulator	1	Z	10 0001 0000 0000
CLRM M	Clear memory M	1	Z	10 0001 1MMM MMMM
COMM M, m	~(M) → (M)	1	Z	10 0010 1MMM MMMM
COMM M, a	~(M) → (acc)	1	Z	10 0010 0MMM MMMM
DECM M, m	Decrement M to M	1	Z	10 0110 1MMM MMMM
DECM M, a	(M) - 1→ (acc)	1	Z	10 0110 0MMM MMMM
DECMSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	10 0111 1MMM MMMM
DECMSZ M, a	(M) - 1→ (acc), skip if (M) = 0	1 + (skip)	None	10 0111 0MMM MMMM
INCM M, m	(M) + 1 → (M)	1	Z	10 1000 1MMM MMMM
INCM M, a	(M) + 1 → (acc)	1	Z	10 1000 0MMM MMMM
INCMSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 + (skip)	None	10 1001 1MMM MMMM
INCMSZ M, a	(M) + 1→ (acc), skip if (M) = 0	1 + (skip)	None	10 1001 0MMM MMMM
IODIR M	Set PA i/o direction	1	None	10 0000 0000 0MMM
IORAM M, m	(M) ior (acc) → (M)	1	Z	10 1111 1MMM MMMM
IORAM M, a	(M) ior (acc) → (acc)	1	Z	10 1111 0MMM MMMM
IORLA I	Literal ior (acc) → (acc)	1	Z	11 0011 iiii iiii
LCALL I	Call subroutine. However, LCALL can addressing 1K address	2	None	01 0iii iiii iiii
LGOTO I	Go branch to any address	2	None	01 1iii iiii iiii
MOVAM m	Move data form acc to memory	1	None	10 0000 1MMM MMMM
MOVLA I	Move literal to accumulator	1	None	11 0001 iiii iiii

MOVM M, m	(M) → (M)	1	Z	10 0011 1MMM MMMM
MOVM M, a	(M) → (acc)	1	Z	10 0011 0MMM MMMM
NOP	No operation	1	None	10 0000 0000 0000
RET	Return	2	None	11 1111 0111 1111
RETI	Return and enable INTM	2	None	11 1111 1111 1111
RETLA I	Return and move literal to accumulator	2	None	11 1100 iiii iiii
RLM M, m	Rotate left from m to itself	1	C	10 1100 1MMM MMMM
RLM M, a	Rotate left from m to acc	1	C	10 1100 0MMM MMMM
RRM M, m	Rotate right from m to itself	1	C	10 1110 1MMM MMMM
RRM M, a	Rotate right from m to acc	1	C	10 1110 0MMM MMMM
SLEEP	Enter sleep (saving) mode	1	$\overline{PD}$	10 0000 0000 0011
SUBAM M, m	(M)–(acc) → (M)	1	C, DC, Z	10 1010 1MMM MMMM
SUBAM M, a	(M)–(acc) → (acc)	1	C, DC, Z	10 1010 0MMM MMMM
SWAPM M, m	Swap data from m to itself	1	None	10 1101 1MMM MMMM
SWAPM M, a	Swap data from m to acc	1	None	10 1101 0MMM MMMM
XORAM M, m	(M) xor (acc) →(M)	1	Z	10 1011 1MMM MMMM
XORAM M, a	(M) xor (acc) →(acc)	1	Z	10 1011 0MMM MMMM
XORLA I	Literal xor (acc) →(acc)	1	Z	11 1000 iiii iiii

9. Electrical characteristics

9.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+3.6V Storge Temperature …….–50℃ to 125℃
Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature…–20℃ to 70℃

9.2 DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		1.8		3.6	V
V_{IH}	Input HighVoltage	3V	I/O Port	2		VDD	V
V_{IL}	Input Low Voltage	3V	I/O Port			0.8	V
I_{DD1}	Standby Current	3V			1		uA
I_{IL}	Input Leakage Current	3V	Vin=VDD, VSS		1		uA
I_{OH}	PortA Driving Current	3V	Voh=2.7V		2.5		mA
			Voh=2.1V		5		
			Voh=1.5V		6.8		
	REM or PC1 Driving Current	3V	Voh=2.7V		2		
			Voh=2.1V		3.7		
			Voh=1.5V		5.1		
I_{OL}	PortA Sink Current	3V	Voh=2.7V		63		uA
			Voh=2.1V		112		
			Voh=1.5V		150		
	REM or PC1 Sink Current	3V	Voh=2.7V		1.6		mA
			Voh=2.1V		2.9		
			Voh=1.5V		3.7		
LV	Low Voltage Reset		LV = 0		2.3		V
R	PortA Pull down resistance	3V	PortA input only		180		KΩ
	PortB or PortC Pull down resistance	3V	PortB or PortC input only		111		KΩ

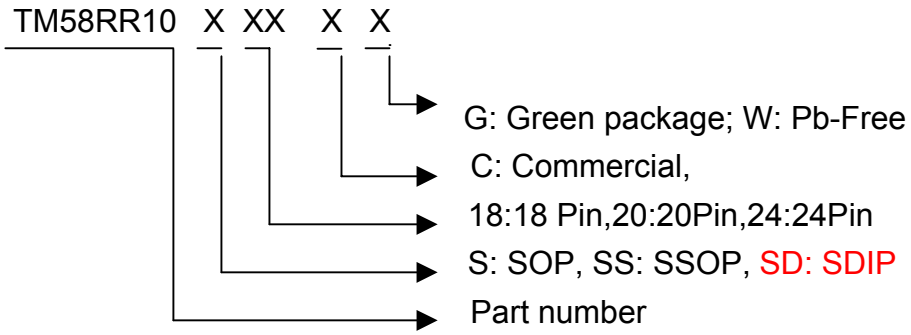
9.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VDD	Conditions				
f_{sys1}	System Clock	3V	NT Crystal mode	200k		10M	hz
T_{rht}	Reset Hold Time		System clk = 4M		250u		s

※ Reset Hold Time = 1000 / System clk

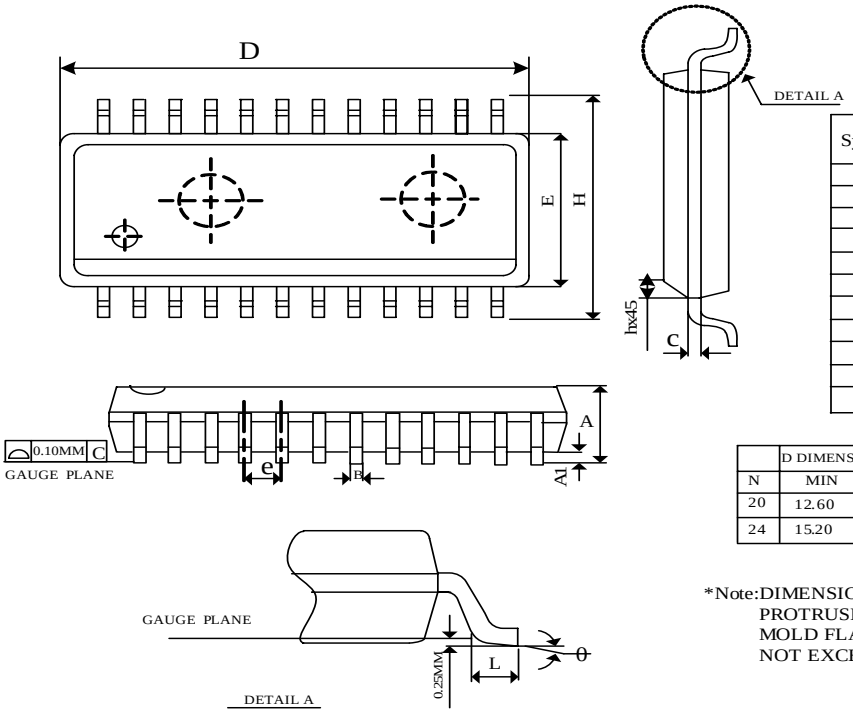
10. Package Information

10.1 Part number Guide



10.2 Package Description

10.2.1 24 , 20pin SOP 300mil

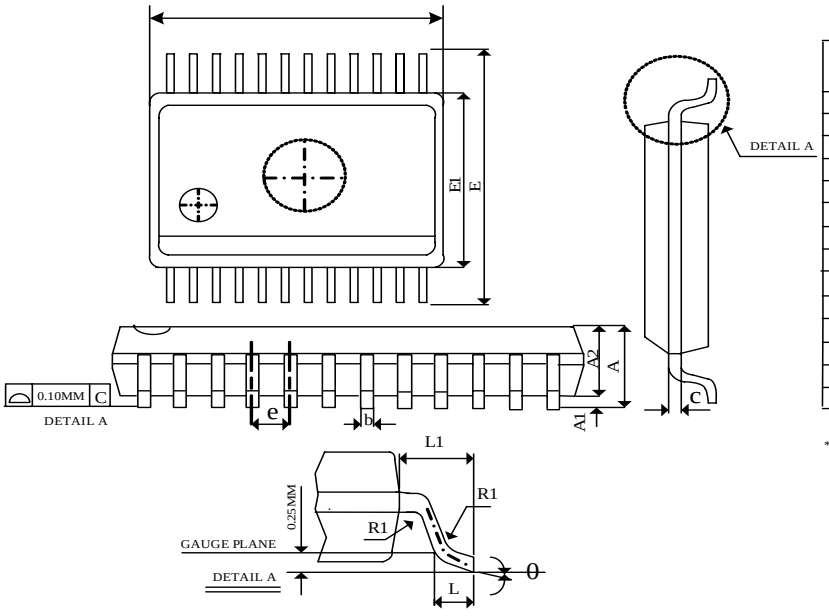


Symbol	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.0091	0.0125
θ	17.70	18.10	0.6969	0.7125
e	1.27 BSC		0.050 BSC	
E	7.40	7.60	0.2914	0.2992
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

	D DIMENSION (IN MM)		D DIMENSION (IN INCH)		
N	MIN	MAX	MIN	MAX	JEDEC
20	12.60	13.00	0.4961	0.5118	MS-013(AC)
24	15.20	15.60	0.5985	0.6141	MS-013(AD)

*Note: DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

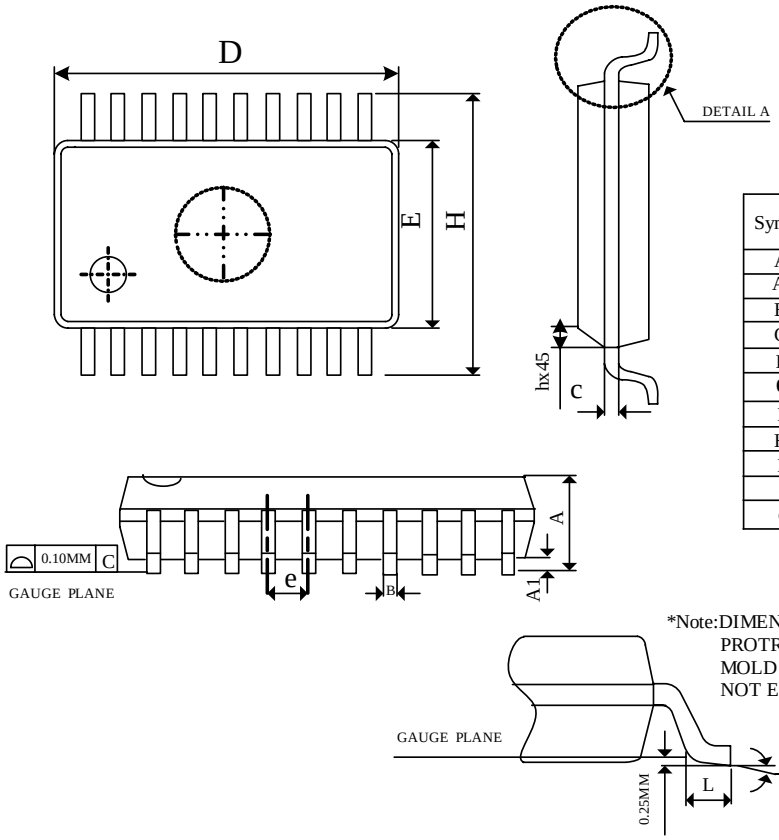
10.2.2 24 pin SSOP 209 mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	
A			2.0			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	0.30	0.33	0.009	0.012	0.013
C	0.09	0.15	0.21	0.004	0.006	0.008
D	9.90	10.20	10.50	0.390	0.402	0.413
e	0.65 BASIC			0.026 BASIC		
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
L	0.55	0.75	0.95	0.022	0.030	0.038
L1	1.25 REF.			0.049 REF.		
R1	0.09			0.004		
θ	D	4	8	0	4	8
JEDEC	MO-150 (AE)					

*Note: DIMENSION "D" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH MOLD FLASH, OR PROTRUSIONS SHALL NOT EXCEED 0.20 MM PER SIDE.

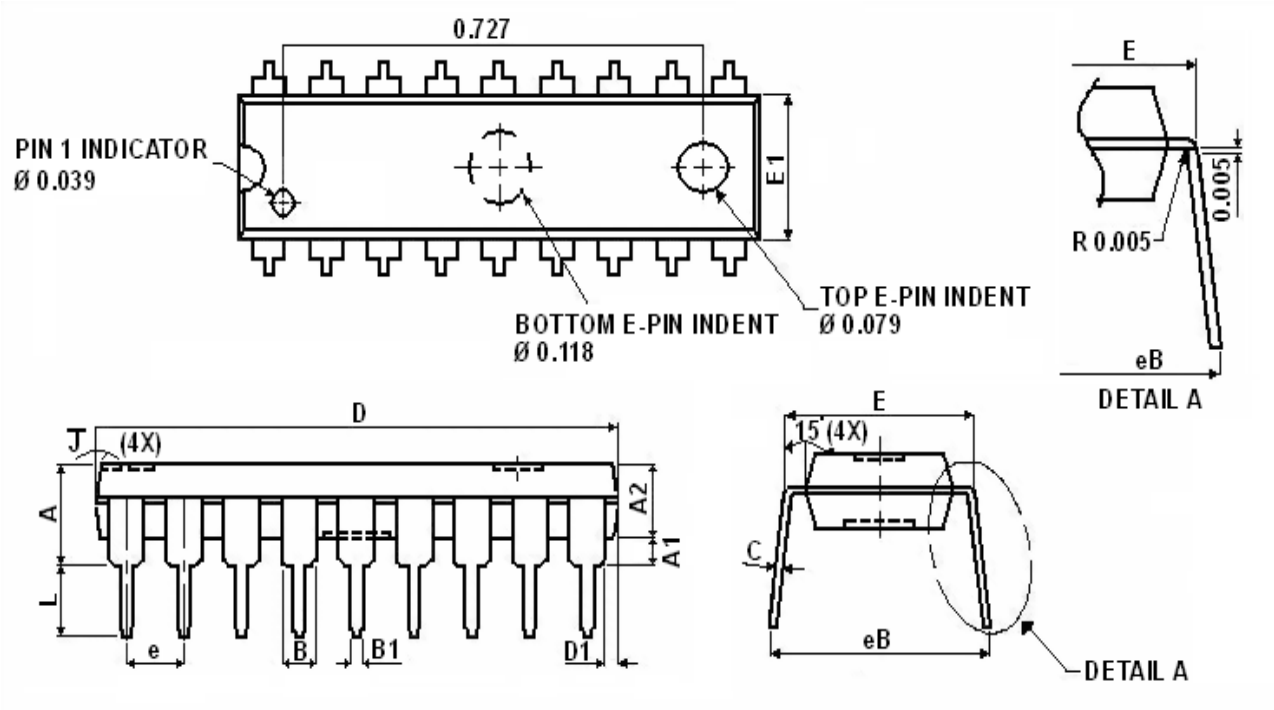
10.2.3 20 pin SSOP 209 mil



Symbol	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.0091	0.0125
D	12.60	13.00	0.4961	0.5118
e	1.27 BSC		0.050 BSC	
E	7.40	7.60	0.2914	0.2992
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

*Note: DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

10.2.4 18 pin DIP 300 mil



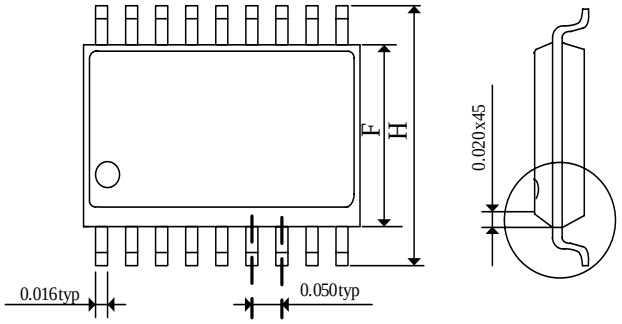
P-DIP 18 PIN-300 MIL

NOTES :

1. **CONTROLLING DIMENSIDN : INCH**
2. PACKAGE DIMENSIDN EXCLLIDE MOLD FLASH OR PROTRUSION
3. **ALLOMABLE MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010”**
4. **FREMA MATERIAL : A194**
5. **TOLERANCE : 0.010” UNLESS OTHERWISE SPECIFIED**
6. **AFTER SOLDER DIPPING LEAD THICKNESS WILL BE 0.020” MAX**

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.57	---	---	0.180
A1	0.38	---	---	0.015	---	---
A2	---	3.30	3.56	---	0.130	0.140
B1	0.36	0.46	0.56	0.014	0.018	0.022
B	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	22.71	22.98	23.11	0.894	0.904	0.910
D1	0.43	0.56	0.69	0.017	0.022	0.027
E	7.62	---	8.26	0.300	---	0.352
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	---	2.54	---	---	0.100	---
L	3.18	---	---	0.125	---	---
eB	8.38	---	9.65	0.330	---	0.380

10.2.5 18pin SOP 300mil



Symbol	MIN	MAX
A	0.093	0.104
A1	0.004	0.012
D	0.447	0.463
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT:INCH

Note:
1. JEDEC OUTLINE: MS-013 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.