十速科技股份有限公司
tenx technology inc.

Advance Information

# TM58RC10

# User Manual

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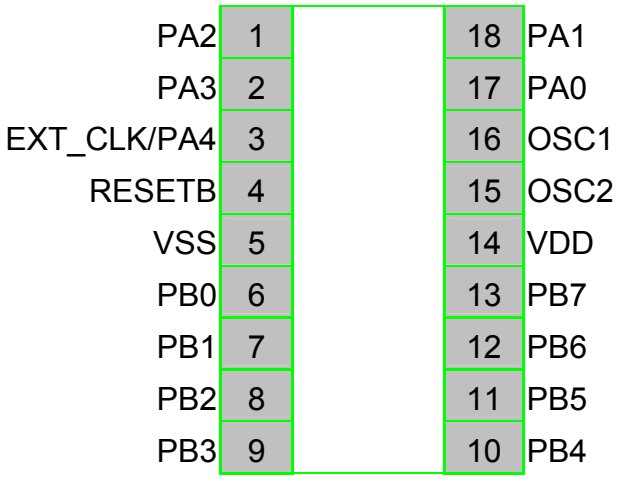
# 目 錄

## 1. Feature

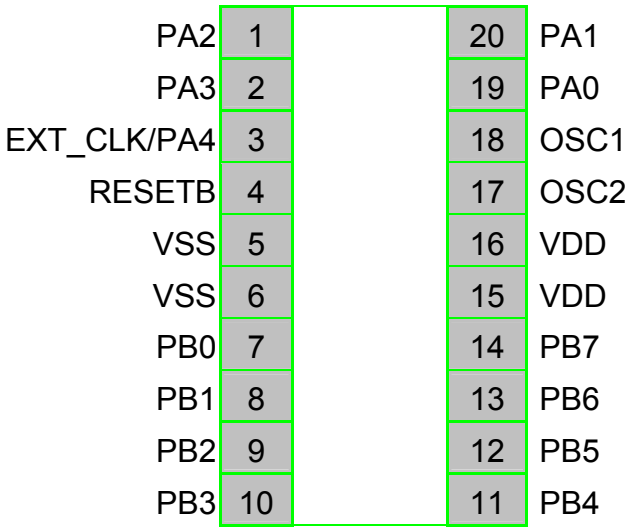
- ROM: 1K x 14 bits
- RAM: 25 x 8 bits
- STACK: 2 Levels
- Two operation modes: General mode and Advanced mode
- Four external Oscillate modes: RC, LP Crystal, NT Crystal and HS Crystal
- I/O ports: 12/13 I/O PAD
- 8 Pull High I/O PAD from Port-B (PULL-Hi resister = 54K (Vdd = 5V))
- 4 normal I/O PAD from Port PA3~A0
- 1 special Input PAD from EXT_CLK/PA4
- Wake-up: Port B pin-change wake-up (Advanced mode only)
- Timer/counter: 8bits x1 (TMR0)
- Prescaler: 3 Bits
- Watchdog Timer: On chip WDT is based on internal RC oscillator. The shortest period is 20mS; user can extend the WDT overflow period to 2.56S by using prescaler.
- Power-On Reset
- Reset Timer: 20 mS (5V)
- Reset mode: (a). Power-On reset
  (b). Low voltage reset
  (c). 1 External Pin reset (RESETB)
  (d). Watchdog timer count overflow reset
- Operation Voltage: 2.2V～5.5V
- Instruction set: 78
- Reset vector: 3FFH
- Package Type: (a). TM58RC10SS20C
  (b). TM58RC10D18C
  (c). TM58RC10S18C
  (d). TM58RC10D14C
  (e). TM58RC10S14C

## 2. Pin Definition & Pad Assignment

### (1). 18 Pin & 20 Pin

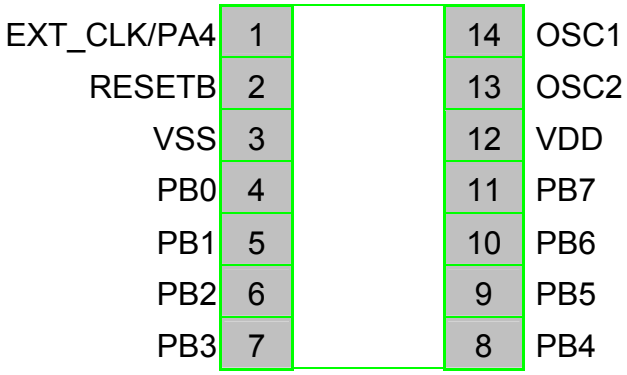



18 Pin Package Types: DIP (TM58RC10D18C)
SOP (TM58RC10S18C)




20Pin Package Type: SSOP (TM58RC10SS20C)

**(2). 14Pin**




14 Pin Package Type: DIP (TM58RC10D14C)
SOP (TM58RC10S14C)

## 3. PIN Description

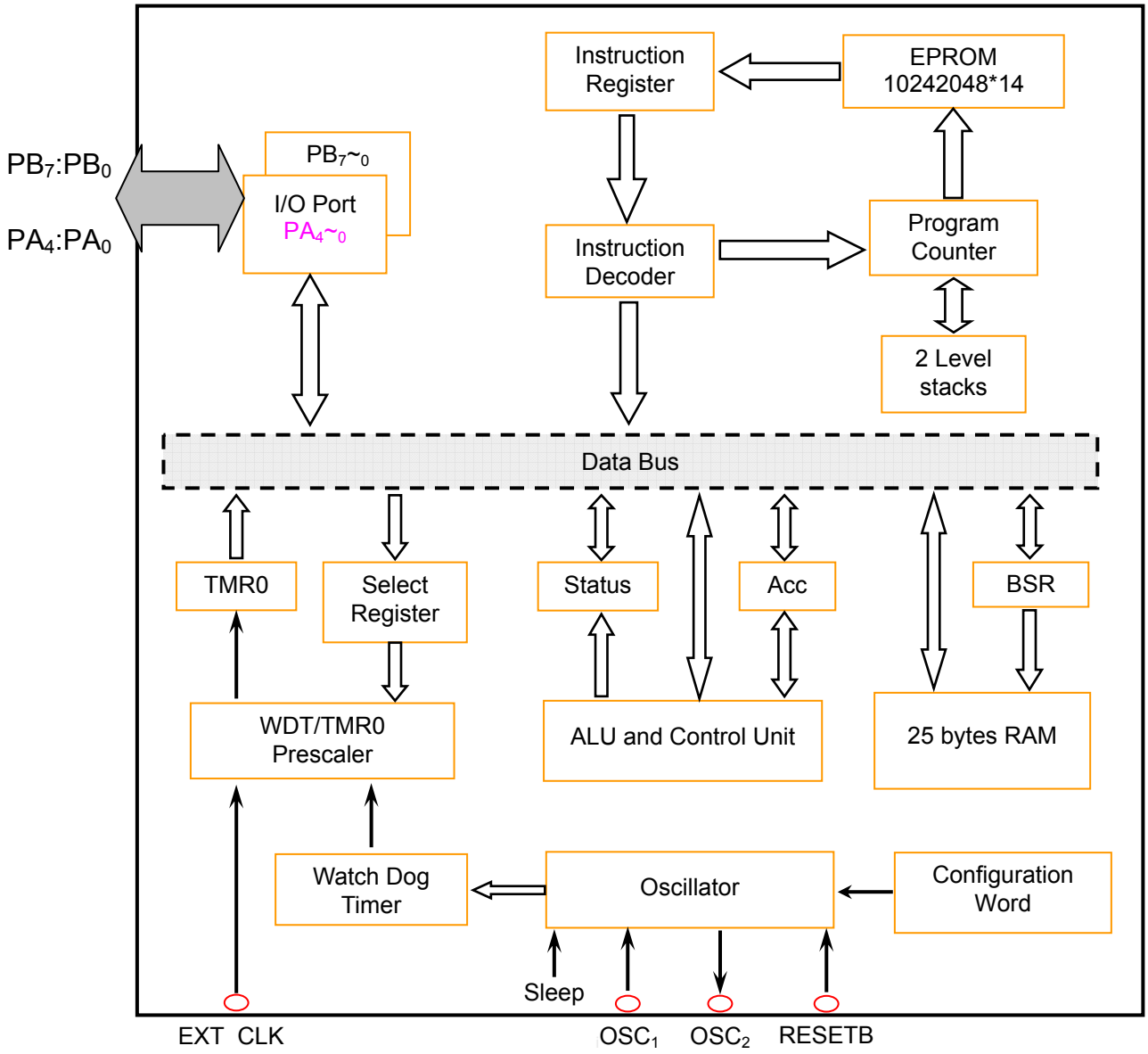
| Pin name | I/O | Description |
|---|---|---|
| EXT_CLK/PA4 | I | 1. External clock input to TMR0 counter<br>2. PA4 input ( When config bit7=1 ) |
| PA3-0 | I/O | I/O port |
| PB7-0 | I/O | 1. I/O port<br>2. Pin-change wake-up (Advanced mode only )<br>3. Pull-UP (Advanced mode only ) |
| RESETB | I | System reset signal |
| OSC1 | I | Oscillator input |
| OSC2 | O | Oscillator output |
| VDD | P | Power input |
| VSS | P | Ground input |

**I: Input; O: Output; I/O: Bi-direction; P: Power**

## 4. Control Register

| Name | Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| CONFIG (Instruction) | | RTCEN | TYPE | LV1 | LV0 | CPT | WDTE | FOSC1 | FOSC0 |
| SELECT | | | | SUR0 | EDGE0 | PSA | PS2 | PS1 | PS0 |
| IAR | $00 | | | | A4 | A3 | A2 | A1 | A0 |
| TMR0 | $01 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PC | $02 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| STATUS | $03 | | | SA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| BSR | $04 | | | | D4 | D3 | D2 | D1 | D0 |
| I/O PortA | $05 | | | | PA4 | PA3 | PA2 | PA1 | PA0 |
| I/O PortB | $06 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |

## 5. System Block Diagram



# 6. Memory Map

TM58RC10 memory is organized into program memory and data memory.

## 6-1. Program memory

TM58RC10 allow directly goto any address in 1K memories without limited by page size. In addition, lcall and lgoto instructions are employed to provide flexible addressing mode. TM58RC10 has a 10-bits program counter capable of accessing 1K spaces. If accessing address has over 1K, then the address will map to physical 1K memories, i.e. 1K+M will be mapped to M. A NOP at the reset vector location will cause a restart at address 000h. A simple map to induce illustrate ROM organization is shown in figures 6-1.

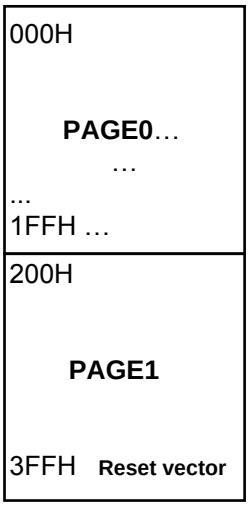



Figure 6-1 The ROM Organization

The configuration word is located 800H that contains OSC selection, WDT enable and code protection. *(Figure 6-2)*.

| Bit | Symbol | Description | | | |
|---|---|---|---|---|---|
| 1~0 | FOSC1~FOSC0 | Bit1 | Bit0 | OSC Type | Resonance Frequency |
| | | 0 | 0 | LP (low speed) | 32~200K Hz |
| | | 0 | 1 | NT(Normal speed) | 200K~10M Hz |
| | | 1 | 0 | HS (high speed) | 10~20M Hz |
| | | 1 | 1 | RC | 32K ~ 6 M Hz |
| 2 | WDTE | WDTE: Watchdog enable/disable control<br>1: WDT enable<br>0: WDT disable | | | |
| 3 | CPT | CPT: Code Protection bit<br>1: OFF<br>0: ON | | | |
| 5~4 | LV1~LV0 | LV1 | LV0 | Detect voltage | |
| | | 0 | 0 | 4V | |
| | | 0 | 1 | Unimplemented | |
| | | 1 | 0 | 2.3V | |
| | | 1 | 1 | Don’t use | |
| 6 | TYPE | TYPE: Select operating mode<br>1: Advanced mode (PB pin-change wakeup )<br>0: General mode | | | |
| 7 | RTCEN | 1 | | PA4 input | |
| | | 0 | | Timer input only | |

**Figure 6-2 The Configuration Word**

### 6-2. Data memory

Data memory is composed of special register and general-purpose ram.
TM58RC10 has 25 general-purpose registers that accessed by using direct or indirect addressing. The special function registers include the program counter (PC), the timer (TMR0) register, the status register, the bank select register, and the I/O port registers. Furthermore, TM58RC10 has 3 auxiliary registers that include indirect addressing register (IAR), the select register (Select) and the I/O direction register (IODIR). The register map is shown in *figure 6-3*.

| | Bank0 |
|---|---|
| 00h | IAR |
| 01h | TMR0 |
| 02h | PC |
| 03h | STATUS |
| 04h | BSR |
| 05h | PORTA |
| 06h | PORTB |
| 9+16=25 | General Purpose Register<br>07 – 0F |
| | General Purpose Register<br>10 -1F |

**Figure 6-3 The Register Map**

The IAR (indirect addressing register) is not a physical register and is used to assist BSR with indirect addressing. Any instruction attempts to access IAR actually mapping to another address that is pointed by BSR. Since IAR is not a material circuit, user reads IAR itself (BSR=00H) will always return 00h at data bus. Writing to IAR itself will like NOP.

Select register is used to control WDT and TMR0. It has not assigned a specific address in data memory and can only set control bits by “select” instruction, i.e. it is write-only register. The context of accumulator will be sent to the select register by executing the “select” instruction. If select register has never set by program, its default value is 3FH. We drew *Figure 6-4* to explain how to set select register.

| Bit | Symbol | Description | | | | |
|---|---|---|---|---|---|---|
| | | PS2 | PS1 | PS0 | TMR0 rate | WDT rate |
| 2~0 | PS2~PS0 | 0 | 0 | 0 | 1:2 | 1:1 |
| | | 0 | 0 | 1 | 1:4 | 1:2 |
| | | 0 | 1 | 0 | 1:8 | 1:4 |
| | | 0 | 1 | 1 | 1:16 | 1:8 |
| | | 1 | 0 | 0 | 1:32 | 1:16 |
| | | 1 | 0 | 1 | 1:64 | 1:32 |
| | | 1 | 1 | 0 | 1:128 | 1:64 |
| | | 1 | 1 | 1 | 1:256 | 1:128 |
| 3 | PSA | PSA: Prescaler assignment bit<br>1: Prescaler assigned to WDT<br>0: Prescaler assigned to TMR0 | | | | |
| 4 | EDGE0 | EDGE0: TMR0 source signal edge control bit<br>1:increment when H→L transition on external clock<br>0:increment when L→H transition on external clock | | | | |
| 5 | SUR0 | SUR0: TMR0 clock source bit<br>1: EXT_CLK clock input<br>0: (System clock)/4 or internal instruction cycle | | | | |

**Figure 6-4 Select Register**

The I/O Direction control register is similar to the Select register that is write-only register. To set an I/O port pin as input, the corresponding direction control bit must be high. Similarly, the zero represents output. Any direction control bit can be programmed individually as input or output by using IODIR instruction. If the register is not programmed, than all I/O ports always keep input mode.

PC (program counter) is a 10-bit wide binary counter and increases itself for every instruction cycle, except the following conditions.

**(1).** call, goto, lgoto and lcall: the label will move to PC

**(2).** retla and ret: the top value of stack will pop to PC

Incrementing PC when it changes to the next higher page. It should be noted that the page select bits in the status register would not be changed synchronously. The following Goto, Call, or MOVAM 02H will return to the previous page, unless the page select bits have been updated in program. In order to reduce the complexity of programming, TM58RC10 provides 2 instructions to facilitate subroutine call and branch handling which are LCALL and LGOTO. LCALL and LGOTO can address to anywhere in the ROM, but the page select bits are unnecessary. The attached operands of CALL and GOTO are 8-bit and 9-bit respectively, and so need extra bits (page select bits) to address whole memory. However, LCALL and LGOTO have 10-bit wide operands that are easy to address the total ROM space.

TMR0 is 8-bit wide binary counter/timer. This register increases by an external signal edge applied to EXT_CLK pin, or by internal instruction cycle. It has the following features.

**(1).** Readable and writeable

**(2).** Synchronize with 2 internal clocks

**(3).** Can use programmable prescaler by setting select register

The other details will be described in follow-up chapter.

Status register contains page select bits, time out bit, power down bit and the status of ALU. Please note that $\overline{TO}$ and $\overline{PD}$ are controlled by hardware and unchangeable by program.

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">0</td><td rowspan="3">C</td><td colspan="2">Carry and $\overline{Borrow}$ bit:</td></tr>
<tr><td>ADD instruction</td><td>SUB instruction</td></tr>
<tr><td>1: a carry occurred from the MSB<br>0: no carry</td><td>1: no borrow (Note1)<br>0: a borrow occurred from the MSB</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">DC</td><td colspan="2">Nibble Carry and Nibble $\overline{Borrow}$ bit</td></tr>
<tr><td>ADD instruction</td><td>SUB instruction</td></tr>
<tr><td>1: a carry from the low nibble bits of the result occurred<br>0: no carry</td><td>1: no borrow<br>0: a borrow from the low nibble bits of the result occurred</td></tr>
<tr><td>2</td><td>Z</td><td colspan="2">Zero bit:<br>1: the result of a logic operation is zero<br>0: the result of a logic operation is not zero</td></tr>
<tr><td>3</td><td>$\overline{PD}$</td><td colspan="2">Power down flag bit: (Note2)<br>1: after power-on or by the CLRWDT instruction<br>0: execute SLEEP instruction</td></tr>
<tr><td>4</td><td>$\overline{TO}$</td><td colspan="2">Time out flag bit:<br>1: after power-on or by the CLRWDT or SLEEP instruction<br>0: Occur WDT time-overflow</td></tr>
<tr><td rowspan="3">5</td><td rowspan="3">SA0</td><td></td><td>Page Location</td></tr>
<tr><td>0</td><td>Page0 (000H~1FFH)</td></tr>
<tr><td>1</td><td>Page1 (200H~3FFH)</td></tr>
</table>

**Figure 6-5 Status Register**

**Note1: A SUB instruction is executed by adding the 2's complement of the subtrahend, so C = 1 represents positive result. The *Figure 6-5-1* show the relation between C-bit and borrow.**

| B0H－50H | | | | | | | | | | 50H－B0H | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | C | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| + | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | + | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| = | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | = | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-5-1**

**Note2: The $\overline{TO}$ and $\overline{PD}$ bits are active low that can be used to determine different causes of reset. The *Figure 6-5-2* illustrates the value of $\overline{TO}$ and $\overline{PD}$ after the relative reset events.**

| $\overline{TO}$ | $\overline{PD}$ | Reset Event |
|---|---|---|
| 0 | 0 | WDT time out from sleep mode |
| 0 | 1 | WDT time out from normal mode |
| 1 | 0 | Input a "Low" at RESETB from sleep mode |
| 1 | 1 | Power on reset |
| Unchanged | Unchanged | Input a "Low" at RESETB from normal |

**Figure 6-5-2**

BSR (bank select register) is associated with IAR to indirectly access the data memory. The BSR<4:0> bits are used to select data memory addresses 00h to 1Fh (Bank0). The addressing map is shown in *Figure 6-6.*

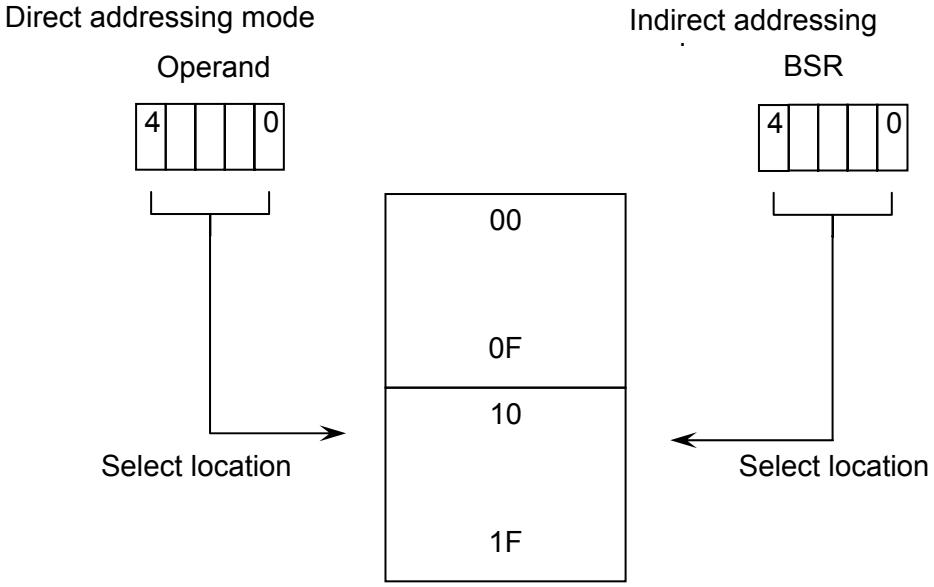



**Figure 6-6 The Direct and Indirect Addressing Map**

Port A~B are programmable I/O ports. Please note that read I/O instruction always read the I/O pin even though the pin is output mode. On reset, all I/O pins were set as input mode until IODIR has been changed.

# 7. Functional Description

## 7-1. TMR0 and Watchdog timer

*Figure 7-1* shows the block diagram of the TMR0/WDT prescaler. As shown in the figure, the prescaler register can be a prescaler for TMR0 or be a postscaler for WDT.

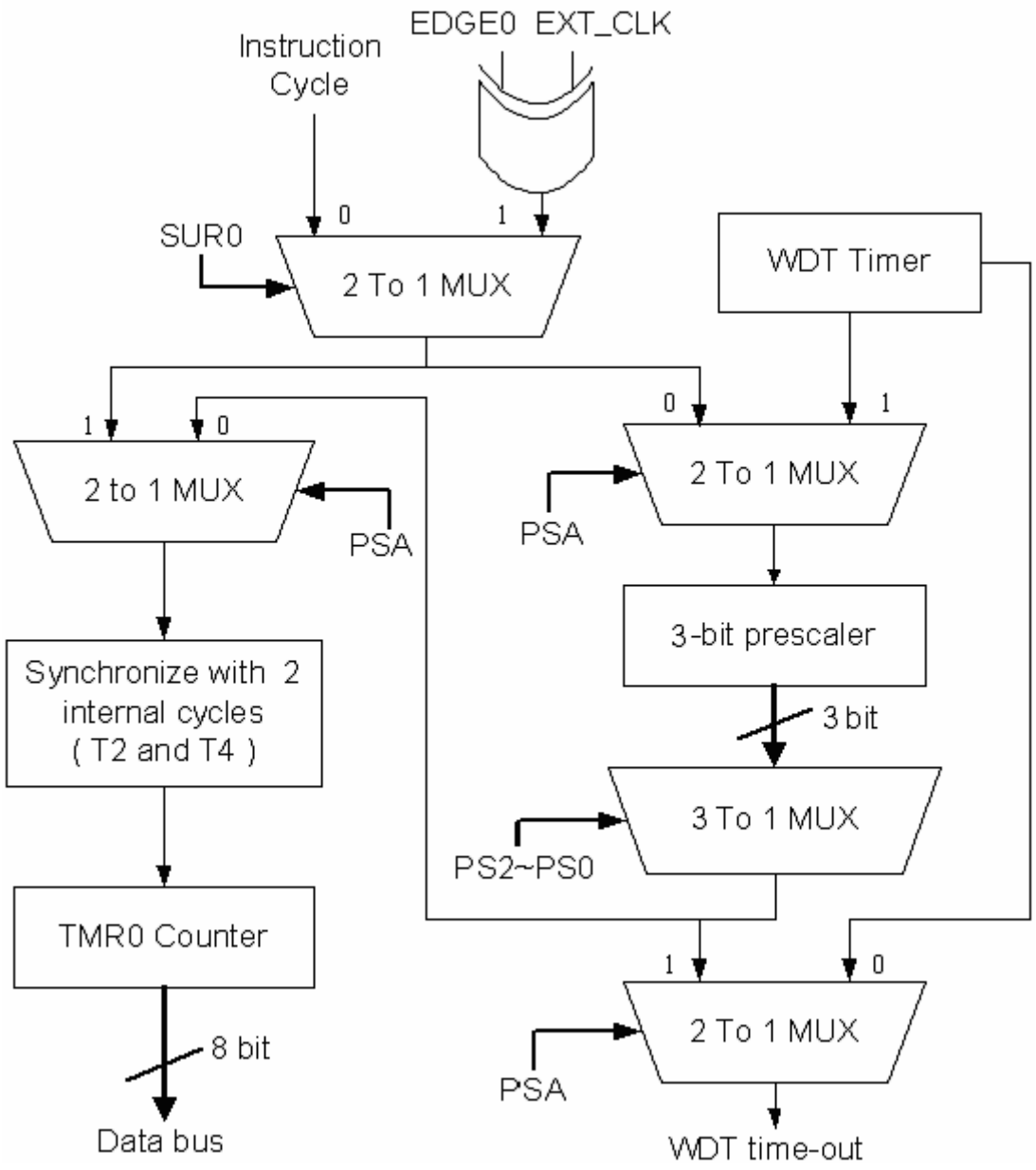



**Figure 7-1 Block Diagram of the TMR0/WDT Prescaler**

The TMR0 is an 8-bit timer/counter. The clock source of TMR0 can come from the instruction clock or the external clock.

To select the instruction clock, the SUR0 bit of the select register should be clear. When no prescaler is used, TMR0 will increase by 1 at every instruction cycle.

To select the external clock, the SUR0 bit of the select register should be set. In this mode, TMR0 relies on the EDGE0 bit to determine that TMR0 is increased by 1 at every falling or rising edge. When an external clock is used for TMR0, a problem must be noted that the external clock synchronizes with internal clock. TM58RC10 synchronizes external clock by sampling internal clock at T2 and T4. If external pulse is smaller than 2 internal cycles, the pulse maybe ignored. Therefore, the external clock must keep stable state (high or low) for at least 2 internal cycles.

The WDT counter is an 8-bit binary counter. The clock source of WDT is provided by an independent on-chip RC oscillator that does not need any external clock. Therefore, the WDT will keep counting even if the chip has slept already. A WDT time-out will restart system and set the time-out flag bit (bit4 of status register) as “0”. The WDT time-out period vary with temperature, power voltage and process. This period can be improved via the prescaler. The maximum division ratio can up to 1:128 by setting PS2~PS0 as “111”.

The prescaler can be assigned to either the TMR0 or the WDT via the PSA bit. Note that either WDT or TMR0 can employ the prescaler simultaneously. The following Example (1-2) must be executed when changing PSA from TMR0 to the WDT and from WDT to the TMR0 respectively. These examples can avoid an unintended time-out reset.

When the prescaler is assigned to WDT, “CLRWDT” and “SLEEP” instruction will clear the prescaler and the WDT. When the prescaler is assigned to TMR0, the prescaler will be cleared by any instruction that writes to TMR0.

```
Clrwdt
Clrm    TMR0        ; clear prescaler & TMR0
Movla   B’00xx1111’
Select
Clrwdt
Movla   B’00xx1xxx’;set prescaler to desired
Select              ; WDT rate
```

Example 1
Changing prescaler from TMR0 to WDT
to WDT

```
Clrwdt    ; clear prescaler & WDT
Movla     B’00xx0xxx’
Select    ; set prescaler to TMR0
          ; with new rate
```

Example 2
Changing prescaler from WDT to TMR0

### 7-2. Reset

TM58RC10 may be reset by one of the following conditions:

**(1).** Power-on.
**(2).** RESETB/VPP pin input a negative pulse.
**(3).** WDT timer out reset (if enable WDTE).
**(4).** Low Voltage reset.

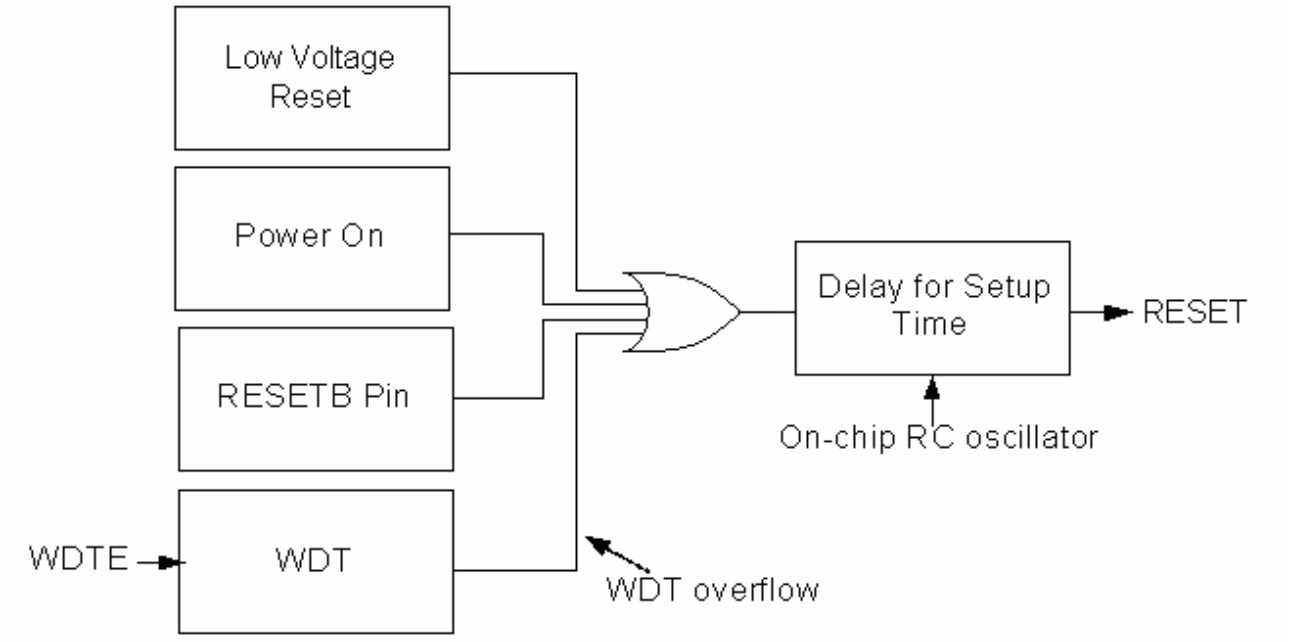



**Figure 7-2 Scheme of the Reset Controller**

As shown in the *figure7-2*, four reset conditions are listed. In general, we call the first and second reset-case as cold reset. The cold reset time may be too short for slow crystals and RC oscillators that require much longer than setup time (note) to oscillate.

**Note: The setup time is approximately 20ms that will affect due to power voltage, process and temperature variations.**

The last two cases are called warm reset. The different reset events will affect registers and ram. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset. These relations are listed in *figure 7-3*.

| Address | Name | Cold Reset | Warm Reset |
|---|---|---|---|
| N/A | Accumulator | xxxx xxxx | pppp pppp |
| N/A | IODIR | 1111 1111 | 1111 1111 |
| N/A | Select | --11 1111 | --11 1111 |
| 00h | IAR | ---- ---- | ---- ---- |

| Address | Name | Cold Reset | Warm Reset |
|---|---|---|---|
| 01h | TMR0 | xxxx xxxx | pppp pppp |
| 02h | PC | 111 1111 1111 | 111 1111 1111 |
| 03h | STATUS | 0001 1xxx | 000? ?ppp |
| 04h | BSR | 111x xxxx | 111p pppp |
| 05h | PORTA | 000x xxxx | 000p pppp |
| 06h | PORTB | xxxx xxxx | pppp pppp |
| | General Purpose RAM | xxxx xxxx | pppp pppp |

### 7-3. RESET CONDITIONS

X: unknown; P: previous data; ?: value depends on condition;
-:unimplemented and read as “0”.

### 7-4. Advanced Mode

In advanced mode, we provide PB7~0 pull-up, PB7~0 wake up functions and PA4 input.
If (TYPE=1) and only if (Port-B Bit [N] as input pin); then Port-B Bit [N] will PULL-Hi and enable wake-up function. ([N] =7~0)

In advanced mode, we provide wake up function. Chip can be wake up from Sleep mode when the logic of the input pin of the Port-B is changed. So we need to read the logic of the input pin before sleep. In advanced mode, the use of a pull-up resistor for the input pin of Port-B. You can set the I/O direction of Port-B by “IODIR” instruction. If the chip wakes up from sleep state, the next instruction of SLEEP will be executed.

Example-1: Wake up

```
Movla     0fh
Iodir     06h        ;; set i/o direction of PORTB
……
Movm      06h,a      ;; read the voltage of the input pin before sleep
sleep                ;; only port-B 3、2、1、0 cab be wakeup
call      delay20ms  ;;this instruction will be executed after wake up
```

The debouche time is the interval that must pass before a second pressing of a key is accepted. User can set this interval with the delay routine (Refer to the Example-1.).

Example 2: Key_Debounche

```
After_wakeup
;-------------------------------------------------------------
int_nt1                     ;; filter out key begin bounce
    btmsc   rb,0
    lgoto   int_nt1
int_loop1                   ;; filter out key end bounce
    call    delay           ;; worse case 30ms
    btmss   rb,0
    lgoto   int_loop1

    call    delay_routine   ;; such as 30ms
    btmss   rb,0
    lgoto   int_loop1
;-----------------------------------
```

## 8. Instruction Set

| Mnemonic Operands | Instruction Code (Advance) | Cycles | Status Affected | OP-code |
|---|---|---|---|---|
| ADDAM M, m | (M)+(acc) → (M) | 1 | C, DC, Z | 10 0101 1MMM MMMM |
| ADDAM M, a | (M)+(acc) → (acc) | 1 | C, DC, Z | 10 0101 0MMM MMMM |
| ANDAM M, m | (M) · (acc) → (M) | 1 | Z | 10 0100 1MMM MMMM |
| ANDAM M, a | (M) · (acc) → (acc) | 1 | Z | 10 0100 0MMM MMMM |
| ANDLA I | Literal · (acc) → (acc) | 1 | Z | 11 1001 iiii iiii |
| BCM M, b0 | Clear bit0 of (M) | 1 | None | 00 1100 0MMM MMMM |
| BCM M, b1 | Clear bit1 of (M) | 1 | None | 00 1100 1MMM MMMM |
| BCM M, b2 | Clear bit2 of (M) | 1 | None | 00 1101 0MMM MMMM |
| BCM M, b3 | Clear bit3 of (M) | 1 | None | 00 1101 1MMM MMMM |
| BCM M, b4 | Clear bit4 of (M) | 1 | None | 00 1110 0MMM MMMM |
| BCM M, b5 | Clear bit5 of (M) | 1 | None | 00 1110 1MMM MMMM |
| BCM M, b6 | Clear bit6 of (M) | 1 | None | 00 1111 0MMM MMMM |
| BCM M, b7 | Clear bit7 of (M) | 1 | None | 00 1111 1MMM MMMM |
| BSM M, b0 | Set bit0 of (M) | 1 | None | 00 1000 0MMM MMMM |
| BSM M, b1 | Set bit1 of (M) | 1 | None | 00 1000 1MMM MMMM |
| BSM M, b2 | Set bit2 of (M) | 1 | None | 00 1001 0MMM MMMM |
| BSM M, b3 | Set bit3 of (M) | 1 | None | 00 1001 1MMM MMMM |
| BSM M, b4 | Set bit4 of (M) | 1 | None | 00 1010 0MMM MMMM |
| BSM M, b5 | Set bit5 of (M) | 1 | None | 00 1010 1MMM MMMM |
| BSM M, b6 | Set bit6 of (M) | 1 | None | 00 1011 0MMM MMMM |
| BSM M, b7 | Set bit7 of (M) | 1 | None | 00 1011 1MMM MMMM |
| BTMSC M, b0 | If bit0 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0100 0MMM MMMM |
| BTMSC M, b1 | If bit1 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0100 1MMM MMMM |
| BTMSC M, b2 | If bit2 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0101 0MMM MMMM |
| BTMSC M, b3 | If bit3 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0101 1MMM MMMM |
| BTMSC M, b4 | If bit4 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0110 0MMM MMMM |
| BTMSC M, b5 | If bit5 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0110 1MMM MMMM |
| BTMSC M, b6 | If bit6 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0111 0MMM MMMM |
| BTMSC M, b7 | If bit7 of (M) = 0, skip next instruction | 1 + (skip) | None | 00 0111 1MMM MMMM |

| Mnemonic Operands | Instruction Code (Advance) | Cycles | Status Affected | OP-code |
|---|---|---|---|---|
| BTMSS M, b0 | If bit0 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0000 0MMM MMMM |
| BTMSS M, b1 | If bit1 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0000 1MMM MMMM |
| BTMSS M, b2 | If bit2 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0001 0MMM MMMM |
| BTMSS M, b3 | If bit3 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0001 1MMM MMMM |
| BTMSS M, b4 | If bit4 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0010 0MMM MMMM |
| BTMSS M, b5 | If bit5 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0010 1MMM MMMM |
| BTMSS M, b6 | If bit6 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0011 0MMM MMMM |
| BTMSS M, b7 | If bit7 of (M) = 1, skip next instruction | 1 + (skip) | None | 00 0011 1MMM MMMM |
| CALL I | Call subroutine | 2 | None | 11 0110 iiii iiii |
| CLRA | Clear accumulator | 1 | Z | 10 0001 0000 0000 |
| CLRM M | Clear memory M | 1 | Z | 10 0001 1MMM MMMM |
| CLRWDT | Clear watch-dog register | 1 | TO, PO | 10 0000 0000 0001 |
| COMM M, m | ~(M) → (M) | 1 | Z | 10 0010 1MMM MMMM |
| COMM M, a | ~(M) → (acc) | 1 | Z | 10 0010 0MMM MMMM |
| DECM M, m | Decrement M to M | 1 | Z | 10 0110 1MMM MMMM |
| DECM M, a | (M) - 1 → (acc) | 1 | Z | 10 0110 0MMM MMMM |
| DECMSZ M, m | (M) - 1 → (M), skip if (M) = 0 | 1 + (skip) | None | 10 0111 1MMM MMMM |
| DECMSZ M, a | (M) - 1 → (acc), skip if (M) = 0 | 1 + (skip) | None | 10 0111 0MMM MMMM |
| GOTO I | Goto branch | 2 | None | 11 101i iiii iiii |
| INCM M, m | (M) + 1 → (M) | 1 | Z | 10 1000 1MMM MMMM |
| INCM M, a | (M) + 1 → (acc) | 1 | Z | 10 1000 0MMM MMMM |
| INCMSZ M, m | (M) + 1 → (M), skip if (M) = 0 | 1 + (skip) | None | 10 1001 1MMM MMMM |
| INCMSZ M, a | (M) + 1 → (acc), skip if (M) = 0 | 1 + (skip) | None | 10 1001 0MMM MMMM |
| IODIR M | Set i/o direction | 1 | None | 10 0000 0000 0MMM |
| IORAM M, m | (M) ior (acc) → (M) | 1 | Z | 10 1111 1MMM MMMM |
| IORAM M, a | (M) ior (acc) → (acc) | 1 | Z | 10 1111 0MMM MMMM |
| IORLA I | Literal ior (acc) → (acc) | 1 | Z | 11 0011 iiii iiii |

| Mnemonic Operands | Instruction Code (Advance) | Cycles | Status Affected | OP-code |
|---|---|---|---|---|
| LCALL I | Call subroutine. However, LCALL can addressing 1K address | 2 | None | 01 0iii iiii iiii |
| LGOTO I | Go branch to any address | 2 | None | 01 1iii iiii iiii |
| MOVAM m | Move data from acc to memory | 1 | None | 10 0000 1MMM MMMM |
| MOVLA I | Move literal to accumulator | 1 | None | 11 0001 iiii iiii |
| MOVM M, m | (M) → (M) | 1 | Z | 10 0011 1MMM MMMM |
| MOVM M, a | (M) → (acc) | 1 | Z | 10 0011 0MMM MMMM |
| NOP | No operation | 1 | None | 10 0000 0000 0000 |
| RET | Return | 2 | None | 11 1111 0111 1111 |
| RETLA I | Return and move literal to accumulator | 2 | None | 11 1100 iiii iiii |
| RLM M, m | Rotate left from m to itself | 1 | C | 10 1100 1MMM MMMM |
| RLM M, a | Rotate left from m to acc | 1 | C | 10 1100 0MMM MMMM |
| RRM M, m | Rotate right from m to itself | 1 | C | 10 1110 1MMM MMMM |
| RRM M, a | Rotate right from m to acc | 1 | C | 10 1110 0MMM MMMM |
| SELECT | Set select register | 1 | None | 10 0000 0000 0010 |
| SLEEP | Enter sleep (saving) mode | 1 | TO, PO | 10 0000 0000 0011 |
| SUBAM M, m | (M)–(acc) → (M) | 1 | C, DC, Z | 10 1010 1MMM MMMM |
| SUBAM M, a | (M) –(acc) → (acc) | 1 | C, DC, Z | 10 1010 0MMM MMMM |
| SWAPM M, m | Swap data from m to itself | 1 | None | 10 1101 1MMM MMMM |
| SWAPM M, a | Swap data from m to acc | 1 | None | 10 1101 0MMM MMMM |
| XORAM M, m | (M) xor (acc) → (M) | 1 | Z | 10 1011 1MMM MMMM |
| XORAM M, a | (M) xor (acc) → (acc) | 1 | Z | 10 1011 0MMM MMMM |
| XORLA I | Literal xor (acc) → (acc) | 1 | Z | 11 1000 iiii iiii |

# 9. Electrical Characteristics

## 9-1. Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V  Storge Temperature ……. –50℃ to 125℃
Input Voltage …… Vss-0.3V to VDD+0.3V  Operating Temperature ….  0℃ to 70℃

## 9-2. DC Characteristics

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | VDD | Conditions | | | | |
| VDD | Operating Voltage | --- | | 2.2 | | 5.5 | V |
| VDVT | Detect Voltage | 5V | Low Voltage Detector (Idd = 3uA) Config bit6.bit5=00 | | 4 | | V |
| | | 3V | Low Voltage Detector (Idd = 1.5uA) Config bit6.bit5=10 | | 2.3 | | V |
| VIL | Input Low Voltage | 5V | I/O Port | | | 0.8 | V |
| IDD1 | Standby Current | 5V | WDT disable | | 1 | | uA |
| | | | WDT enable | | 10 | | |
| IIL | Input Leakage Current | 5V | Vin=VDD, VSS | | 1 | | uA |
| IDD1 | Standby Current | 5V | LVD disable,WDT disable,LV disable | | 1 | | uA |
| | | 5V | LVD disable,WDT enable,LV disable | | 5 | | uA |
| | | 3V | LVD disable,WDT disable,LV disable | | 1 | | uA |
| | | 3V | LVD disable,WDT enable,LV disable | | 2 | | uA |
| IIL | Input Leakage Current | 5V | Vin=VDD, VSS | | 1 | | uA |
| | | | Vol=01V | | 35 | | |
| | | | Vol=1.5V | | 50 | | |
| RPUHI | Pull_Hi Pin Resister | 5V | Set PortB input pin and Pull_Hi | | 60 | | KΩ |
| | | 3V | Set PortB input pin and Pull_Hi | | 150 | | |

### 9-3. AC Characteristics

| Symbol | Parameter | Test Conditions | | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | VDD | Conditions | | | | |
| $f_{sys1}$ | System Clock | 5V | LP Crystal mode | 32 | | 200 | Khz |
| | | 3V | | 32 | | 200 | |
| $f_{sys2}$ | System Clock | 5V | NT Crystal mode | 0.2 | | 10 | Mhz |
| | | 3V | | 0.2 | | 10 | |
| $f_{sys3}$ | System Clock | 5V | HS Crystal mode | 10 | | 20 | Mhz |
| | | 3V | | | | | |
| $f_{sys4}$ | System Clock | 5V | RC mode | | | 6 | Mhz |
| | | 3V | | | | 6 | |
| $T_{wdt}$ | Watchdog Timer | 5V | | | 20 | | mS |
| | | 3V | | | 25 | | |
| $T_{rht}$ | Reset Hold Time | 5V | | | 20 | | mS |
| | | 3V | | | 25 | | |

### 9-4. External RC Tables

RC 頻率表(5V, 25℃), Sample S1~S6

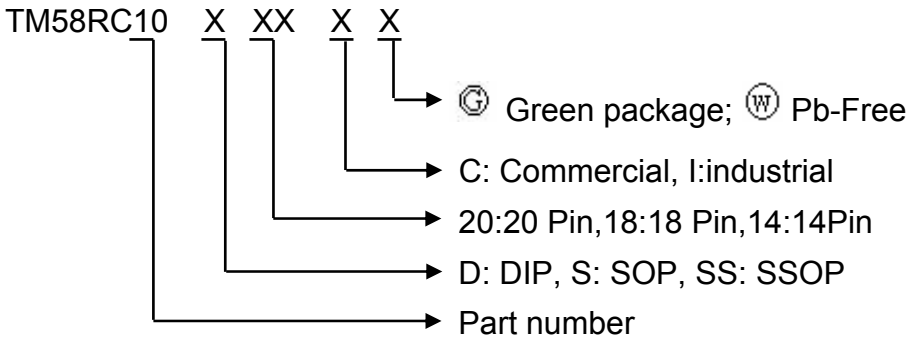
| R | C | S1 | S2 | S3 | S4 | S5 | S6 | Freq(unit) |
|---|---|---|---|---|---|---|---|---|
| 7.5M | 0.1u | 24.37 | 25.59 | 27.38 | 26.00 | 27.35 | 25.82 | K Hz |
| | 20p | 25.10 | 26.08 | 27.61 | 26.48 | 27.54 | 26.33 | |
| | **PS(1)** | 25.21 | 26.25 | 27.88 | 26.64 | 27.67 | 26.43 | |
| 6M | 0.1u | 30.39 | 31.96 | 34.10 | 32.76 | 34.07 | 32.30 | |
| | 20p | 31.40 | 32.66 | 34.38 | 33.07 | 34.33 | 32.96 | |
| | -- | 31.63 | 32.88 | 34.81 | 33.36 | 34.58 | 33.17 | |
| 330K | 0.1u | 395.4 | 402.1 | 407.3 | 405.2 | 408.0 | 406.3 | |
| | 20p | 407.0 | 413.2 | 417.7 | 416.0 | 417.6 | 417.0 | |
| | -- | 421.7 | 427.8 | 433.8 | 430.5 | 432.1 | 431.1 | |
| 300K | 0.1u | 449.7 | 456.8 | 463.6 | 460.4 | 463.6 | 461.2 | |
| | 20p | 463.3 | 469.5 | 476.0 | 472.6 | 474.7 | 473.2 | |
| | -- | 480.4 | 486.5 | 494.4 | 489.7 | 491.4 | 489.8 | |
| 150K | 0.1u | 0.878 | 0.886 | 0.902 | 0.892 | 0.896 | 0.892 | M Hz |
| | 20p | 0.905 | 0.912 | 0.929 | 0.918 | 0.920 | 0.916 | |
| | -- | 0.939 | 0.946 | 0.964 | 0.951 | 0.953 | 0.949 | |
| 120K | 0.1u | 1.125 | 1.134 | 1.153 | 1.141 | 1.144 | 1.139 | |
| | 20p | 1.163 | 1.171 | 1.192 | 1.178 | 1.179 | 1.175 | |
| | -- | 1.203 | 1.211 | 1.233 | 1.218 | 1.217 | 1.214 | |
| 75K | 0.1u | 1.808 | 1.818 | 1.847 | 1.829 | 1.826 | 1.823 | |
| | 20p | 1.882 | 1.890 | 1.921 | 1.902 | 1.896 | 1.893 | |
| | -- | 1.951 | 1.959 | 1.992 | 1.969 | 1.958 | 1.958 | |
| 68K | 0.1u | 2.004 | 2.013 | 2.044 | 2.025 | 2.021 | 2.018 | |
| | 20p | 2.088 | 2.095 | 2.129 | 2.109 | 2.100 | 2.098 | |
| | -- | 2.162 | 2.169 | 2.203 | 2.181 | 2.170 | 2.170 | |
| 39K | 0.1u | 3.551 | 3.559 | 3.608 | 3.581 | 3.556 | 3.559 | |
| | 20p | 3.753 | 3.755 | 3.807 | 3.775 | 3.743 | 3.748 | |
| | -- | 3.935 | 3.939 | 3.993 | 3.954 | 3.917 | 3.916 | |
| 36K | 0.1u | 3.865 | 3.868 | 3.921 | 3.891 | 3.864 | 3.867 | |
| | 20p | 4.076 | 4.080 | 4.134 | 4.103 | 4.065 | 4.070 | |
| | -- | 4.275 | 4.278 | 4.334 | 4.295 | 4.255 | 4.253 | |

VDD = 5V

| R | C | S1 | S2 | S3 | S4 | S5 | S6 | Freq(unit) |
|---|---|---|---|---|---|---|---|---|
| 20K | 0.1u | 7.323 | 7.313 | 7.399 | 7.349 | 7.270 | 7.281 | M Hz |
| | 20p | 7.849 | 7.833 | 7.921 | 7.861 | 7.758 | 7.770 | |
| | -- | 8.137 | 8.114 | 8.195 | 8.141 | 8.041 | 8.048 | |
| 18K | 0.1u | 8.185 | 8.169 | 8.260 | 8.208 | 8.112 | 8.125 | |
| | 20p | 8.770 | 8.745 | 8.840 | 8.775 | 8.669 | 8.679 | |
| | -- | 9.087 | 9.056 | 9.147 | 9.080 | 8.964 | 8.973 | |

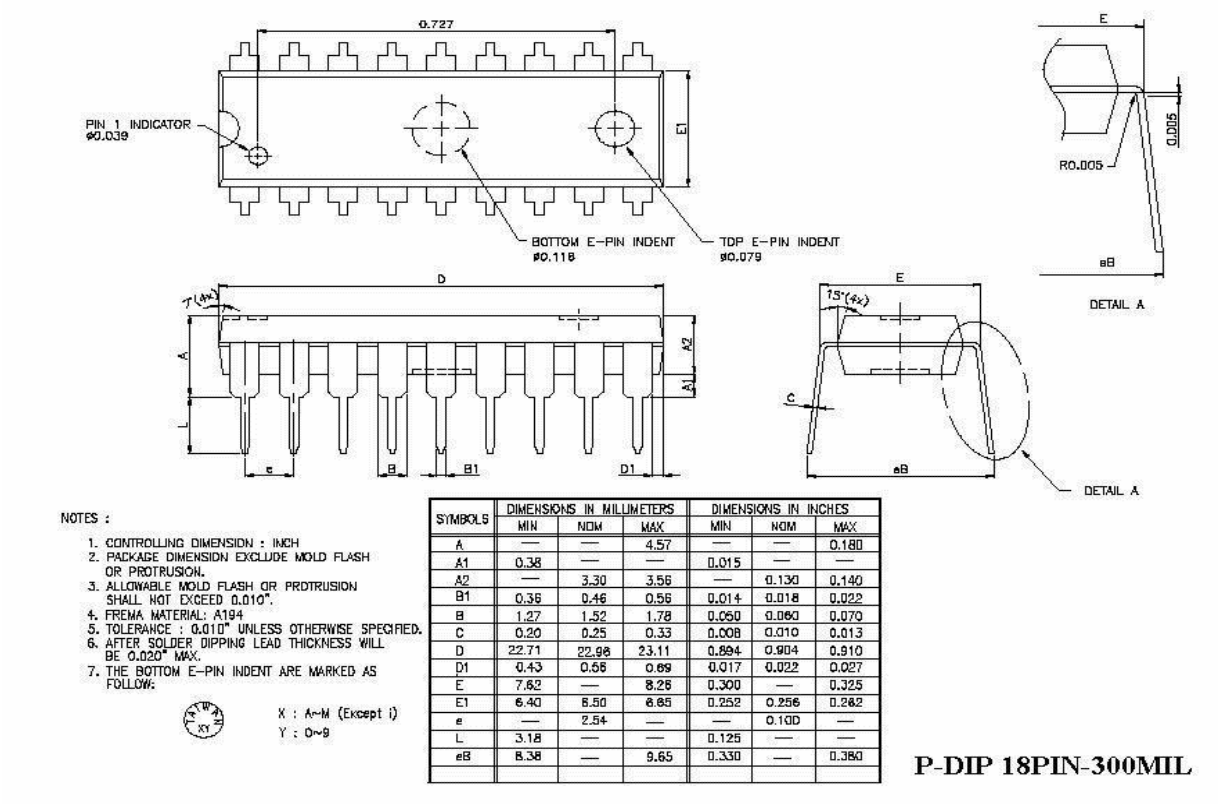
**Note-1: No capacitor.**

## 10. Part number Guide



## 10-1. Package mode

**(1).** 18Pin DIP (300 mil)




NOTES :

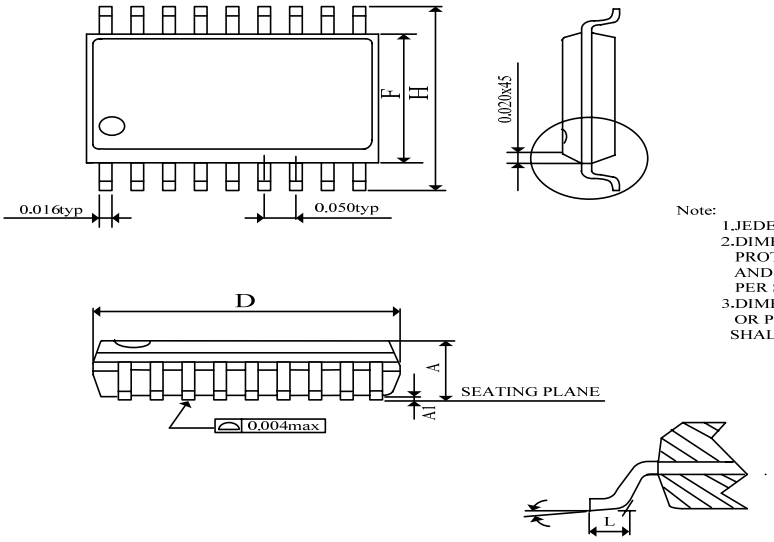
1. CONTROLLING DIMENSION : INCH
2. PACKAGE DIMENSION EXCLUDE MOLD FLASH OR PROTRUSION.
3. ALLOWABLE MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010".
4. FREMA MATERIAL: A194
5. TOLERANCE : 0.010" UNLESS OTHERWISE SPECIFIED.
6. AFTER SOLDER DIPPING LEAD THICKNESS WILL BE 0.020" MAX.
7. THE BOTTOM E-PIN INDENT ARE MARKED AS FOLLOW:

X : A~M (Except i)
Y : 0~9

| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 4.57 | — | — | 0.180 |
| A1 | 0.38 | — | — | 0.015 | — | — |
| A2 | — | 3.30 | 3.56 | — | 0.130 | 0.140 |
| B1 | 0.36 | 0.46 | 0.56 | 0.014 | 0.018 | 0.022 |
| B | 1.27 | 1.52 | 1.78 | 0.050 | 0.060 | 0.070 |
| C | 0.20 | 0.25 | 0.33 | 0.008 | 0.010 | 0.013 |
| D | 22.71 | 22.98 | 23.11 | 0.894 | 0.904 | 0.910 |
| D1 | 0.43 | 0.56 | 0.69 | 0.017 | 0.022 | 0.027 |
| E | 7.62 | — | 8.26 | 0.300 | — | 0.325 |
| E1 | 6.40 | 6.50 | 6.65 | 0.252 | 0.256 | 0.262 |
| e | — | 2.54 | — | — | 0.100 | — |
| L | 3.18 | — | — | 0.125 | — | — |
| eB | 8.38 | — | 9.65 | 0.330 | — | 0.380 |

P-DIP 18PIN-300MIL

**(2).** 18Pin SOP (300 mil)

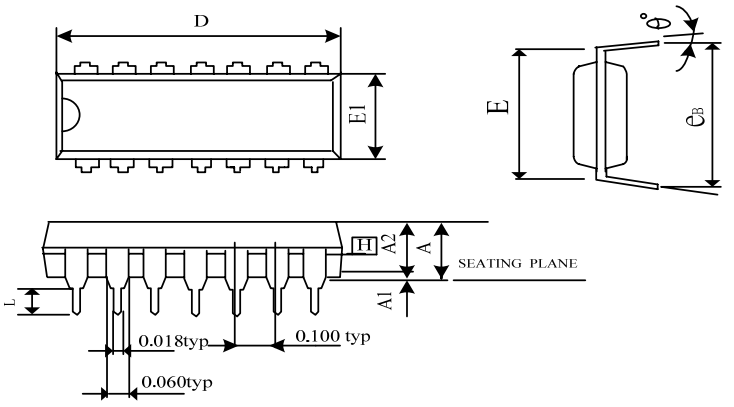



| Symbol | MIN | MAX |
|---|---|---|
| A | 0.093 | 0.104 |
| A1 | 0.004 | 0.012 |
| D | 0.447 | 0.463 |
| E | 0.291 | 0.299 |
| H | 0.394 | 0.419 |
| L | 0.016 | 0.050 |
| θ° | 0 | 8 |

UNIT:INCH

Note:
1.JEDEC OUTLINE:MS-013 AB
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm(.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm(.010in) PER SIDE.

**(3).** 14Pin DIP (300 mil)



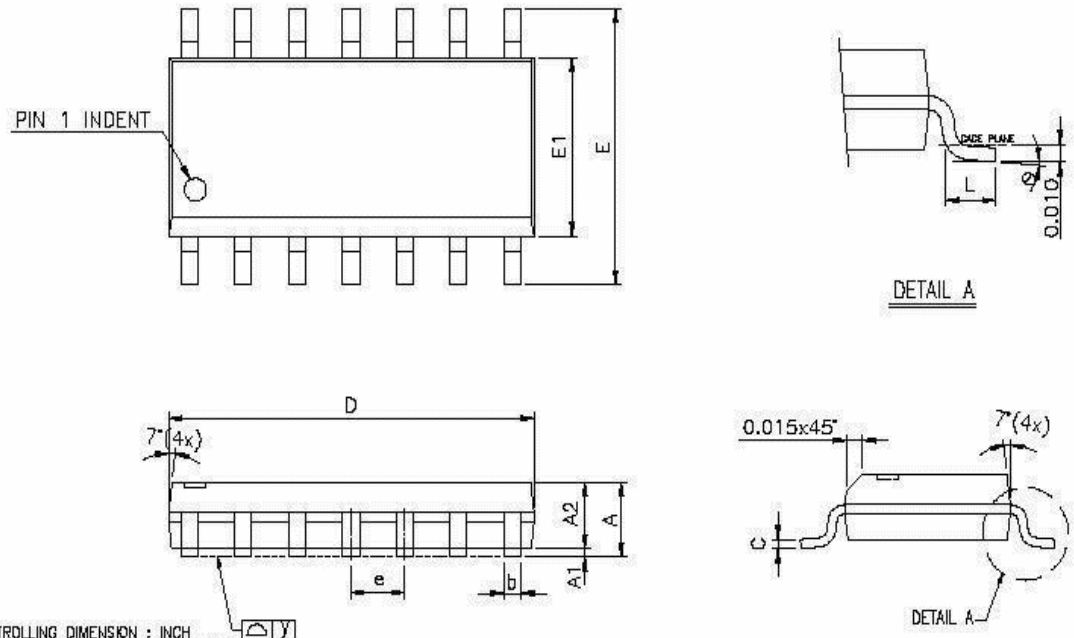

| SYMBOLS | MIN | NOR | MAX |
|---|---|---|---|
| A | — | — | 0.210 |
| A1 | 0.015 | — | — |
| A2 | 0.125 | 0.130 | 0.135 |
| D | 0.735 | 0.750 | 0.775 |
| E | | 0.300 BSC | |
| E1 | 0.245 | 0.250 | 0.255 |
| L | 0.115 | 0.130 | 0.150 |
| eB | 0.335 | 0.355 | 0.375 |
| θ° | 0 | 7 | 15 |

UNIT : INCH

NOTES:
1.JEDEC OUTLINE:MS-001 AA

3.eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4.POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5.DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINNUM.
6.DATUM PLANE H COINCIDENT WITH THE BOTTON OF LEAD,WHERE LEAD EXITS BODY.

**(4).** 14Pin SOP (150 mil)

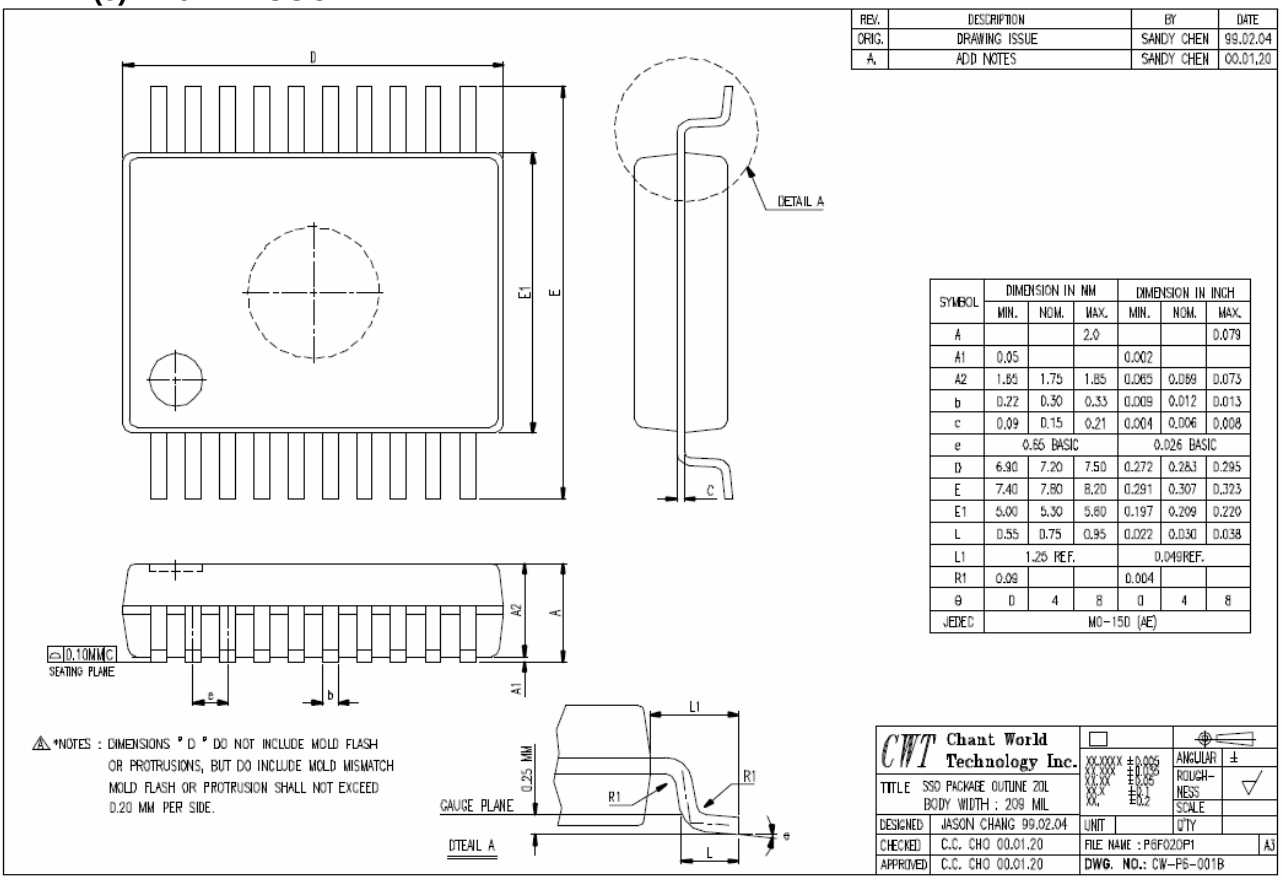



NOTE :
1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.47 | 1.60 | 1.73 | 0.058 | 0.063 | 0.068 |
| A1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 |
| A2 | — | 1.45 | — | — | 0.057 | — |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| C | 0.19 | 0.20 | 0.25 | 0.0075 | 0.008 | 0.0098 |
| D | 8.53 | 8.64 | 8.74 | 0.336 | 0.340 | 0.344 |
| E | 5.79 | 5.99 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.81 | 3.91 | 3.99 | 0.150 | 0.154 | 0.157 |
| e | — | 1.27 | — | — | 0.050 | — |
| L | 0.38 | 0.71 | 1.27 | 0.015 | 0.028 | 0.050 |
| y | — | — | 0.076 | — | — | 0.003 |
| θ | 0° | — | 8° | 0° | — | 8° |

SOP-14PIN-150MIL

**(5).** 20 PIN SSOP




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 2.0 | | | 0.079 |
| A1 | 0.05 | | | 0.002 | | |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| b | 0.22 | 0.30 | 0.33 | 0.009 | 0.012 | 0.013 |
| c | 0.09 | 0.15 | 0.21 | 0.004 | 0.006 | 0.008 |
| e | 0.65 BASIC | | | 0.026 BASIC | | |
| D | 6.90 | 7.20 | 7.50 | 0.272 | 0.283 | 0.295 |
| E | 7.40 | 7.80 | 8.20 | 0.291 | 0.307 | 0.323 |
| E1 | 5.00 | 5.30 | 5.60 | 0.197 | 0.209 | 0.220 |
| L | 0.55 | 0.75 | 0.95 | 0.022 | 0.030 | 0.038 |
| L1 | 1.25 REF. | | | 0.049REF. | | |
| R1 | 0.09 | | | 0.004 | | |
| θ | 0 | 4 | 8 | 0 | 4 | 8 |
| JEDEC | MO-150 (AE) | | | | | |