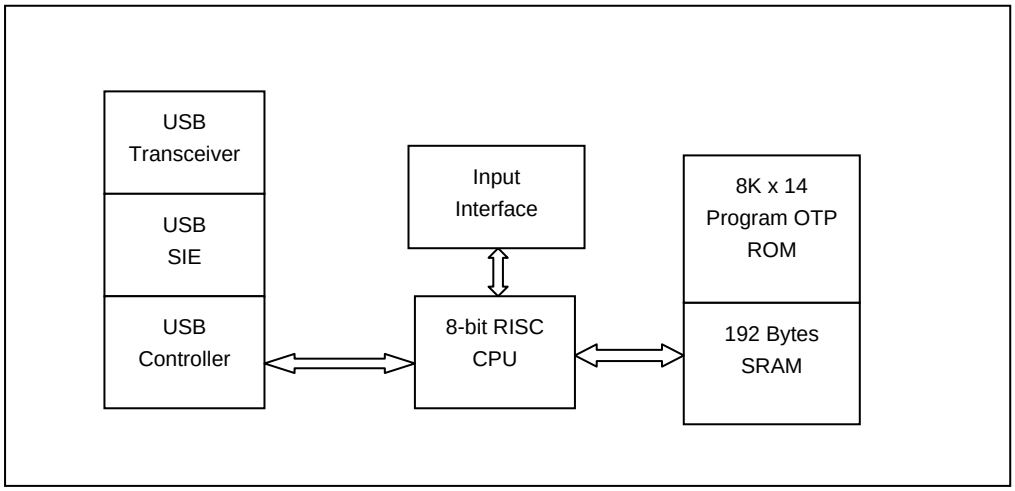
The TMU3101 is an 8-bit microprocessor embedded device tailored to the USB/PS2 Mouse application. It includes an 8-bit RISC CPU core, 192-byte SRAM, Low Speed USB Interface and an 8K x 14 internal program OTP-ROM.

FEATURE

- Compliance with the Universal Serial Bus specification v1.1
- Built-in USB Transceiver without external pull-up resister and 3.3V regulator
- Support USB Suspend and Resume function
- One Control IN/OUT and one Interrupt IN endpoints
- PS2 compatible mouse interface share with USB interface
- 192 byte internal SRAM
- 8K x 14 internal program OTP-ROM
- 8-bit RISC CPU core with only 36 instruction
- 3MHz instruction rate with 6MHz crystal oscillation
- Support internal wake up timer for power saving.
- 18/20/24 pin PDIP/SOP package

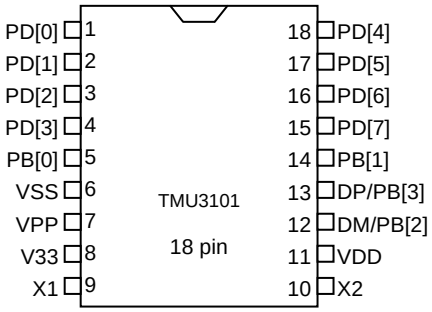
BLOCK DIAGRAM

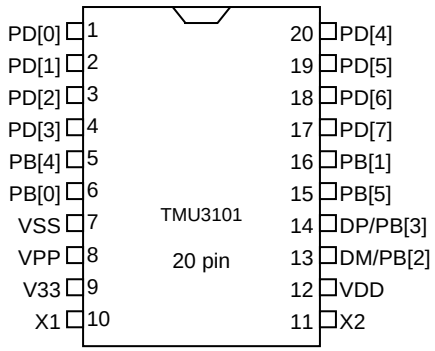


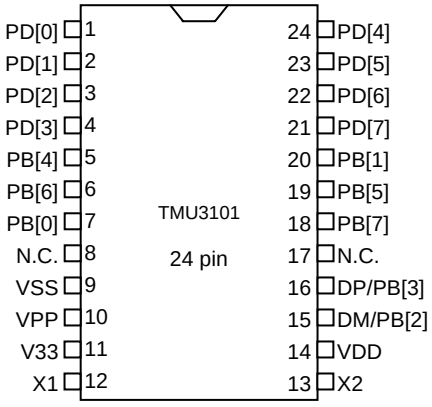
PIN DESCRIPTION

Name	I/O	Description
VDD	P	5V Power from USB cable
VSS	P	Ground
X1	I	Crystal in (6MHz)
X2	O	Crystal out
VPP	I	OTP programming power
V33	O	3.3V regulator output
DP/PB[3]	I/O	USB positive data signal / General purpose I/O (pseudo open-drain)
DM/PB[2]	I/O	USB negative data signal / General purpose I/O (pseudo open-drain)
PB[1:0]/ PB[7:4]	I/O	General purpose I/O (pseudo open-drain)
PD[7:0]	I/O	Multi-function I/O (pseudo open-drain, Push-pull output, Input from pin or comparator.)

PIN ASSIGNMENT







FUNCTIONAL DESCRIPTION

1. CPU Core

1.1 Clock Scheme and Instruction Cycle

The clock input (X1) is internally divided by two to generate Q1 state and Q2 state for each instruction cycle. The Programming Counter (PC) is updated at Q1 and the instruction is fetched from program ROM and latched into the instruction register in Q2. It is then decoded and executed during the following Q1-Q2 cycle.

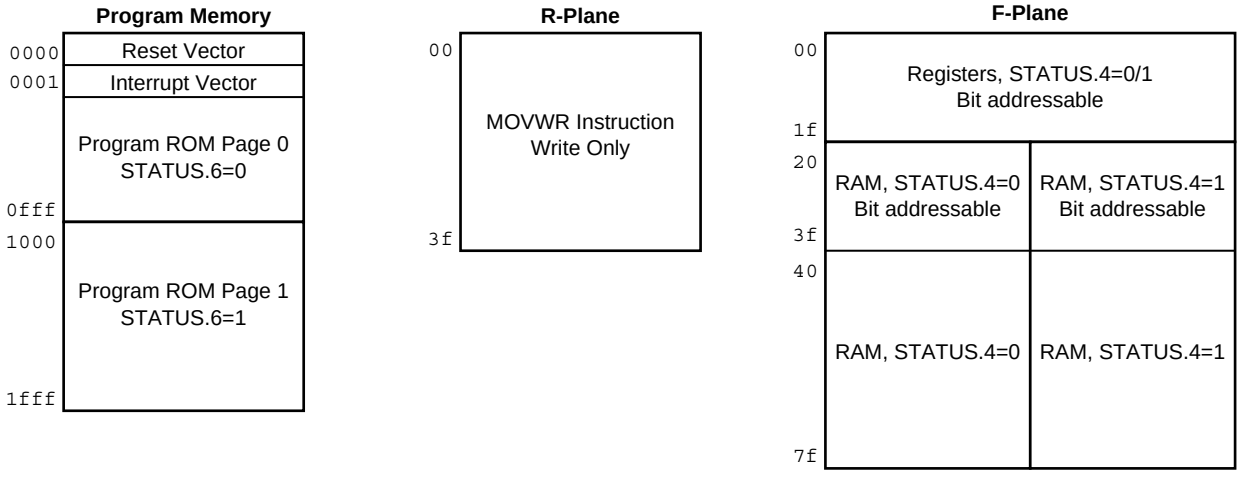
1.2 Programming Counter (PC) and Stack

The Programming Counter is 13-bit wide capable of addressing a 8K x 14 program ROM. As a program instruction is executed, the PC will contain the address of the next program instruction to be executed. The PC value is normally increased by one except the followings. The Reset Vector (0) and the Interrupt Vector (1) are provided for PC initialization. For CALL/GOTO instructions, PC loads its lower 12 bits from instruction word and the MSB from STATUS's bit 6. For RET/RETI/RETLW instructions, PC retrieves its content from the top level STACK. For the other instructions updating PC[7:0], the PC[12:8] keeps unchanged.

The STACK is 13-bit wide and 6-level in depth. The CALL instruction and Hardware interrupt will push STACK level in order, While the RET/RETI/RETLW instruction pops the STACK level in order.

1.3 Addressing Mode

There are two Data Memory Plane in CPU, R-Plane and F-Plane. The registers in R-Plane are write-only. The "MOVWR" instruction copy the W-register's content to those registers by direct addressing mode. Registers in F-Plane can be addressed directly or indirectly. Indirect Addressing is made by address "0", where FSR points to an actual address. The first half of F-Plane is also bit-addressable.



1.4 ALU and Working (W) Register

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. In two-operand instructions, typically one operand is the W register, which is an 8-bit non-addressable register used for ALU operations. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either W register or a file register.

Depending on the instruction executed, the ALU may affect the values of Carry(C), Digit Carry(DC), and Zero(Z) Flags in the STATUS register. The C and DC flags operate as a /Borrow and /Digit Borrow, respectively, in subtraction.

1.5 STATUS Register

This register contains the arithmetic status of ALU and the page select for Program ROM and Data RAM. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect those bits.

1.6 Interrupt

Each interrupt source has its own enable control bit. An interrupt event will set its individual flag. If the corresponding interrupt enable bit has been set, it would trigger CPU to service the interrupt. CPU accepts interrupt in the end of current executed instruction cycle. In the mean while, A “CALL 0001” instruction is inserted to CPU, and the I-flag is set to prevent recursive interrupt nesting. The I-flag is cleared in the instruction after the “RETI” instruction. That is, at least one instruction in main program is executed before service the pending interrupt. The interrupt event is level trigged. F/W must clear the interrupt event register while serves the interrupt routine.

1.7 Instruction Set

Each instruction is a 14-bit word divided into an OPCODE, which specified the instruction type, and one or more operands, which further specify the operation of the instruction. The instructions can be categorized as byte-oriented, bit-oriented and literal operations list in the following table.

For byte-oriented instructions, “f” represents address designator and “d” represents destination designator. The address designator is used to specify which address in F-Plane is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If “d” is “0”, the result is placed in the W register. If “d” is “1”, the result is placed in the address specified in the instruction.

For bit-oriented instructions, “b” represents a bit field designator, which selects the number of the bit affected by the operation, while “f” represents the address designator.

For literal operations, “k” represents the literal or constant value.

For “MOVWR” instruction, “r” specifies which address in R-Plane is to be used by the instruction.

All instructions are single cycle except for program branches, which are two-cycle.

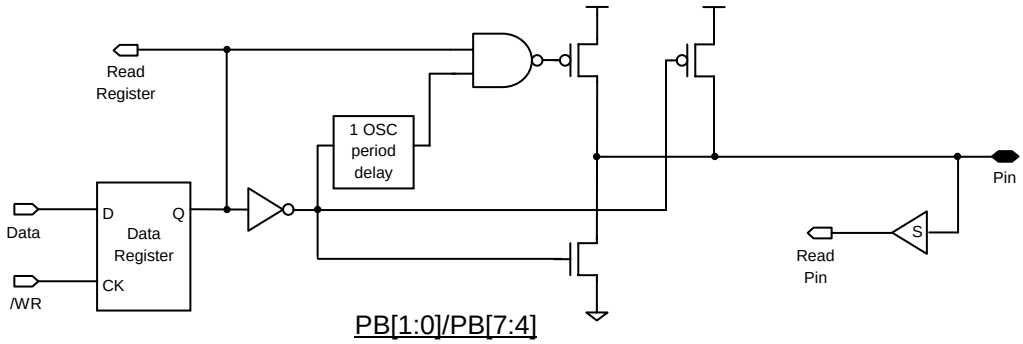
Mnemonic	Op Code	Cycles	Flag Affect	Description
NOP	00 0000 0 0000000	1	-	No operation
SLEEP	00 0000 0 0000011	1		Go into standby mode, Clock oscillation stops
CLRWDT	00 0000 0 0000100	1		Clear and enable Watch Dog Timer
MOVWR r	00 0000 0 0rrrrrr	1	-	Move W to “r”
RET	00 0000 0 1000000	2	-	Return
RETI	00 0000 0 1100000	2	-	Return from interrupt
MOVWF f	00 0000 1 fffffff	1	-	Move W to “f”
CLRW	00 0001 0 1000000	1	Z	Clear W
CLRF f	00 0001 1 fffffff	1	Z	Clear “f”
SUBWF f,d	00 0010 d fffffff	1	C,DC,Z	Subtract W from “f”
DECF f,d	00 0011 d fffffff	1	Z	Decrement “f”
IORWF f,d	00 0100 d fffffff	1	Z	OR W with “f”
ANDWF f,d	00 0101 d fffffff	1	Z	AND W with “f”
XORWF f,d	00 0110 d fffffff	1	Z	XOR W with “f”
ADDWF f,d	00 0111 d fffffff	1	C,DC,Z	Add W and “f”
MOVFW f	00 1000 0 fffffff	1	-	Move “f” to “w”
TESTZ f	00 1000 1 fffffff	1	Z	Test if “f” is zero
COMF f,d	00 1001 d fffffff	1	Z	Complement “f”
INCF f,d	00 1010 d fffffff	1	Z	Increment “f”
DECFSZ f,d	00 1011 d fffffff	1 or 2	-	Decrement “f”, skip if zero
RRF f,d	00 1100 d fffffff	1	C	Rotate right “f” through carry
RLF f,d	00 1101 d fffffff	1	C	Rotate left “f” through carry
SWAPF f,d	00 1110 d fffffff	1	-	Swap high/low nibble of “f”
INCFSZ f,d	00 1111 d fffffff	1 or 2	-	Increment “f”, skip if zero
BCF f,b	010 00 bbb ffffff	1	-	Clear “b” bit of “f”
BSF f,b	010 01 bbb ffffff	1	-	Set “b” bit of “f”
BTFSC f,b	010 10 bbb ffffff	1 or 2	-	Test “b” bit of “f”, skip if clear
BTFSS f,b	010 11 bbb ffffff	1 or 2	-	Test “b” bit of “f”, skip if set
RETLW k	011 000 kkkkkkkk	2	-	Return, place Literal “k” in W
MOVLW k	011 001 kkkkkkkk	1	-	Move Literal “k” to W
IORLW k	011 010 kkkkkkkk	1	Z	OR Literal “k” with W
ANDLW k	011 011 kkkkkkkk	1	Z	AND Literal “k” with W
ADDLW k	011 100 kkkkkkkk	1	C,DC,Z	Add Literal “k” to W
XORLW k	011 111 kkkkkkkk	1	Z	XOR Literal “k” with W
CALL k	10 kkkk kkkkkkkk	2	-	Call subroutine “k”
GOTO k	11 kkkk kkkkkkkk	2	-	Jump to branch “k”

2. I/O Port

2.1 PB[1:0]/PB[7:4]

These pins are “Pseudo-Open-Drain” structure. In “Read-Modify-Write” instruction, CPU actually reads the output data register. In the others instructions, CPU reads the pin data. The so-called “Read-Modify-Write” instruction includes BSF, BCF and all instructions using F-Plane as destination.

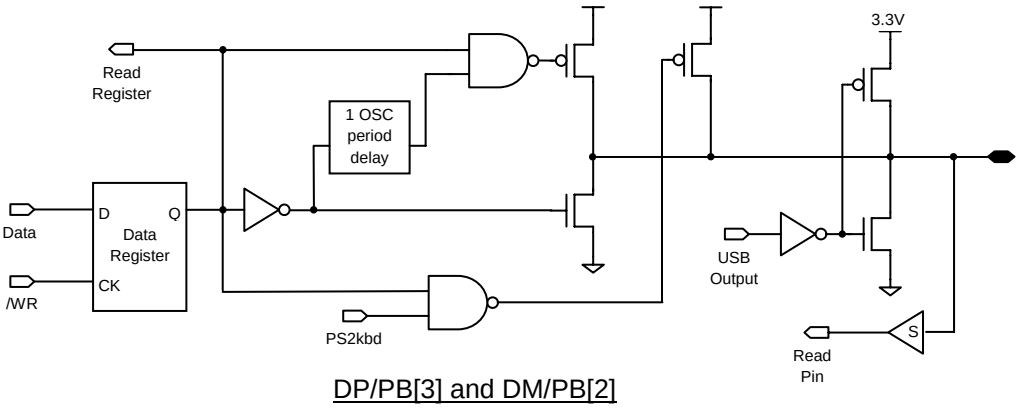
The PB[0] pin can also generate interrupt (PB0int) at its falling edge.



PB[1:0]/PB[7:4]

2.2 DP/PB[3] and DM/PB[2]

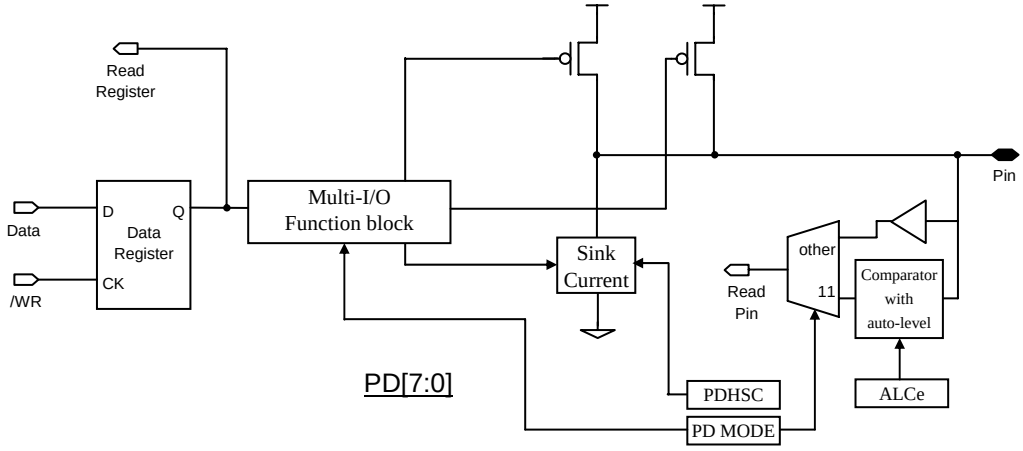
These pins are similar to PB[1:0], except they share the pin with USB function. An extra control bit “PS2kbd” is used to enable the small pull-up current.



DP/PB[3] and DM/PB[2]

2.3 PD[7:0]

The attributions of I/O pins are defined to be multi-function for adapting different application. The PD MODE defines the I/O type as below. If is “pseudo open drain” structure, the function are similar to PB, only different is sink capability, the sink capability of pin can be control form corresponding PDHSC register. The read path can be read from output data latch or pin data. About the comparator with auto-level function is very suitable for mouse application, PD[0]/PD[1] must be grouped to mapping X1/X2 or Y1/Y2, PD[2]/PD[3] also must mapping the rest axis. When PD[3:0] operating on comparator with auto level function, this ALCe register must be set, clear ALCe register to disable this function for saving power.



2.4 Electrical Characterisitics of IO Ports

PD[7:0] I/O type	PD MODE	Output		Read	Note
		HIGH	LOW		
Pseudo open drain	00	5mA->30uA	PDHSC=0, Low Sink	Output data register or pin data	PD[5:0]: Low sink=8mA, High sink=30mA
Push-pull output	01	4mA	PDHSC=1, High Sink	Output data register	PD[7:6]: Low sink=16mA High sink=50mA
Input, read from pin	10	N.A.	N.A.	Pin data	
Input, read from comparator	11	N.A	N.A.	Pin data	PD[7:4] unavailable

3. Power Down Mode

The power down mode is activated by SLEEP instruction. In power down mode, the crystal clock oscillation stops to minimize power consumption. Power down mode can be terminated by Reset or enabled Interrupts.

4. Watch Dog Timer

The Watch Dog Timer (WDT) is disabled after Reset. F/W can use the CLRWDT instruction to clear and enable the Watch Dog Timer. Once enabled, the Watch Dog Timer overflow and generate a chip reset signal if no CLRWDT executed in a period of 4000000 oscillator's cycle (0.66 second for 6MHz crystal). The WDT does not work in Power Down Mode to provide wake-up function. It is only designed to prevent F/W goes into endless loop.

5. Timer 0

The Timer 0 is an 8-bit wide register of F-Plane. It can be read or written as any other register of F-Plane. Besides, Timer 0 increases itself periodically and reloads itself with a special value every time while roll over. The value to be load at roll over point is defined by "Timer 0 Reload" (T0RLD) register in the R-Plane. The period which Timer 0 increases itself is defined by "Timer 0 Pre-Scale" (T0PSCL) register in R-Plane. The Timer 0 also generates interrupt (T0int) while it rolls over.

6. Internal Wakeup Timer

TMU3101 is built-in a nonstop internal RC oscillator whose period is around 50ms. It may be used for periodic polling TMU3101 on mouse application. While enter power down mode, crystal clock oscillation is stop. If enable the WKT interrupt, when wakeup timer overflow will generate wakeup interrupt and WKTint=1. Write any to CLRWKT register can clear this wakeup timer.

7. USB Engine

The USB engine includes the Serial Interface Engine (SIE), the low-speed USB I/O transceiver and the 3.3 Volt Regulator. The SIE block performs most of the USB interface function with only minimum support from F/W. Three endpoints are supported. Endpoint 0 is used to receive and transmit control (including SETUP) packets while Endpoint 1 is only used to transmit data packets.

The USB SIE handles the following USB bus activity independently:

1. Bitstuffing/unstuffing
2. CRC generation/checking
3. ACK/NAK
4. TOKEN type identification
5. Address checking

F/W handles the following tasks:

1. Coordinate enumeration by responding to SETUP packets
2. Fill and empty the FIFOs
3. Suspend/Resume coordination
4. Verify and select DATA toggle values

7.1 USB Device Address

The USB device address register (USBadr) stores the device's address. This register is reset to all 0 after chip reset. F/W must write this register a valid value after the USB enumeration process.

7.2 Endpoint 0 receive

After receiving a packet and placing the data into the Endpoint 0 receive FIFO (RC0FIFO), TMU3101 updates the Endpoint 0 status registers to record the receive status and then generates an Endpoint 0 receive interrupt (RC0int). F/W can read the status register for the recent transfer information, which includes the data byte count (RC0cnt), data direction (EP0dir), SETUP token flag (EP0set), packet toggle (RC0tgl) and data valid flag (RC0err). The received data is always stored into RC0FIFO and the RC0cnt is always updated for DATA packets following SETUP tokens. The data following an OUT token is written into the RC0FIFO, and the RC0cnt is updated unless Endpoint 0 STALL (EP0stall) is set or Endpoint 0 receive ready

(RC0rdy) is cleared. The SIE clears the RC0rdy automatically and generates RC0int interrupt when the RC0cnt or RC0FIFO is updated. As long as the RC0rdy is cleared, SIE keep responding NAK to Host's Endpoint 0 OUT packet request. F/W should set the RC0rdy flag after the RC0int interrupt is asserted and RC0FIFO is read out.

7.3 Endpoint 0 transmit

After detecting a valid Endpoint 0 IN token, TMU3101 automatically transmit the data pre-stored in the Endpoint 0 transmit FIFO (TX0FIFO) to the USB bus if the Endpoint 0 transmit ready flag (TX0rdy) is set and the EP0stall is cleared. The number of byte to be transmitted depends on the Endpoint 0 transmit byte count register (TX0cnt). The DATA0/1 token to be transmitted depends on the Endpoint 0 transmit toggle control bit (TX0tgl). After the TX0FIFO is updated, TX0rdy should be set to 1. This enables the TMU3101 to respond to an Endpoint 0 IN packet. TX0rdy is cleared and an Endpoint 0 transmit interrupt (TX0int) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX0rdy to confirm that the data transfer was successful.

7.4 Endpoint 1 transmit

Endpoint1 is capable of transmit only. These endpoints are enabled when the Endpoint1 configuration control bit (EP1cfg) is set. After detecting a valid Endpoint 1 IN token, TMU3101 automatically transmit the data pre-stored in the Endpoint 1 transmit FIFO (TX1FIFO) to the USB bus if the Endpoint 1 transmit ready flag (TX1rdy) is set and the EP1stall is cleared. The number of byte to be transmitted depends on the Endpoint 1 transmit byte count register (TX1cnt). The DATA0/1 token to be transmitted depends on the Endpoint 1 transmit toggle control bit (TX1tgl). After the TX1FIFO is updated, TX1rdy should be set to 1. This enables the TMU3101 to respond to an Endpoint 1 IN packet. TX1rdy is cleared and an Endpoint 1 transmit interrupt (TX1int) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX1rdy to confirm that the data transfer was successful.

7.5 USB Control and Status

Other USB control bits include the USB enable (ENUSB), Suspend (Susp), Resume output (RsmO), Control Read (CtrRD), and corresponding interrupt enable bits. The CtrRD should be set when program detects the current transfer is an Endpoint0 Control Read Transfer. Once this bit is set, the TMU3101 will stall an Endpoint0 OUT packet with DATA toggle 0 or byte count other than 0. Other USB status flag includes the USB reset interrupt (RSTint), Resume input interrupt (RSMint), and USB Suspend interrupt (SUSPint).

7.6 Suspend and Resume

Once the Suspend condition is asserted, F/W can set the Susp bit to save the power consumption of USB Engine. F/W can further save the device power by force the CPU to go into the Power Down Mode. In the Power Down mode, the X'tal is stop, but CPU can be waken-up by the trigger of enabled interrupt's source, which includes RSMint, KBDint and PB0int.

The TMU3101 send Resume signaling to USB bus when Susp=1 and RsmO=1. In the suspend mode, if a valid interrupt is asserted, F/W should send resume signal to wake up the USB bus.

Some PCs send Reset wakeup instead of Resume under Suspend condition, TMU3101 will first service RSMint, at the same time RSTint flag is set after several clocks.

8. MEMORY MAP

8.1 MEMORY MAP of F-Plane

Name	Address	R/W	Rst	Description
Timer0	01.7~0	R/W	0	Timer 0
PCL	02.7~0	R/W	0	Program Counter [7~0]
ROMpage	03.6	R/W	0	Program ROM Page Select (STATUS.6)
RAMbank	03.4	R/W	0	SRAM Bank Select (STATUS.4)
Z	03.2	R/W	0	Zero Flag (STATUS.2)
DC	03.1	R/W	0	Decimal Carry Flag or Decimal /Borrow Flag (STATUS.1)
C	03.0	R/W	0	Carry Flag or /Borrow Flag (STATUS.0)
FSR	04.6~0	R/W	0	File Select Register to define Address in indirect addressing mode
PBD	06.7~0	R/W	ff	Port B output datalatch / pin
PDD	0D.7~0	R/W	ff	Port D output datalatch / pin / comparator dataindata
GPR0	0E.7~0	R/W	-	General Purpose Register 0
GPR1	0F.7~0	R/W	-	General Purpose Register 1
ENUSB	10.7	R/W	0	USB function enable (1)
USBadr	10.6~0	R/W	0	USB device address
RC0int	11.7	R/W	0	Endpoint 0 Receive Interrupt flag, write 0 to clear flag.
TX0int	11.6	R/W	0	Endpoint 0 Transmit Interrupt flag, write 0 to clear flag.
TX1int	11.5	R/W	0	Endpoint 1 Transmit Interrupt flag, write 0 to clear flag.
RSTint	11.3	R/W	0	USB Bus Reset Interrupt flag, write 0 to clear flag.
SUSPint	11.2	R/W	0	USB Suspend Interrupt flag, write 0 to clear flag.
WKTint	11.1	R/W	0	Wake-up timer (50ms) Interrupt flag, write 0 to clear flag.
RSMint	12.3	R/W	0	USB Resume Interrupt flag, write 0 to clear flag.
PB0int	12.1	R/W	0	PB0 interrupt flag, write 0 to clear flag.
T0int	12.0	R/W	0	Timer0 Interrupt flag, write 0 to clear flag.
Susp	13.7	R/W	0	F/W force USB interface to go into suspend mode.
RsmO	13.6	R/W	0	F/W force USB interface send Resume signal in suspend mode.
EP1cfg	13.5	R/W	0	Set Endpoint 1 configuration.
CtrRD	13.3	R/W	0	H/W will stall an invalid OUT token during Control Read transfer.
RC0rdy	13.0	R/W	0	Endpoint 0 ready for receive, clear by H/W while RC0int occurs.
RC0tgl	14.7	R		1: received DATA1 packet; 0: received DATA0 Packet.
RC0err	14.6	R		Endpoint 0 received data error.
EP0dir	14.5	R		1: IN transfer; 0: OUT/SETUP transfer.
EP0set	14.4	R		SETUP Token indicator.
RC0cnt	14.3~0	R		Received data byte count.
TX0rdy	15.7	R/W	0	Endpoint 0 ready for transmit, clear by H/W while TX0int occurs.
TX0tgl	15.6	R/W	0	Endpoint 0 transmit DATA1/DATA0 packet.
EP0stall	15.5	R/W	0	Endpoint 0 will stall OUT/IN packet while this bit is 1.
TX0cnt	15.3~0	R/W	0	Endpoint 0 transmit byte count.
TX1rdy	16.7	R/W	0	Endpoint 1 ready for transmit, clear by H/W while TX1int occurs.
TX1tgl	16.6	R/W	0	Endpoint 1 transmit DATA1/DATA0 packet.
EP1stall	16.5	R/W	0	Endpoint 1 will stall IN packet while this bit is 1.
TX1cnt	16.3~0	R/W	0	Endpoint 1 transmit byte count.
RC0FIFO	18~1F	R		Endpoint 0 Receive Buffer (8 Bytes)
SRAM	20~7F	R/W	-	Internal RAM (96 Bytes x 2 Banks)

8.2 MEMORY MAP of R-Plane

Name	Address	R/W	Rst	Description
T0RLD	01.7~0	W	0	Timer0 overflow reload value
T0PSCL	02.3~0	W	0	Timer0 Pre-Scale, 0:divided by 2, 1:divided by 4, … 7:divided by 256, 8:divided by 1 , Time base is 2*instruction cycle
PWRdwn	03	W	0	Write this register to enter Power-Down Mode
WDTe	04	W	0	Write this register to clear WDT and enable WDT
CLRWKT	08	W	0	Write this register to clear Wake-up Timer
PDHSC	0E.7~0	W	0	Port D pin in High sink current mode, PD[7:6]:16mA/50mA, PD[5:0]:8mA/30mA
PD7MODE	0D.7~6	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin
PD6MODE	0D.5~4	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin
PD5MODE	0D.3~2	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin
PD4MODE	0D.1~0	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin
PD3MODE	0C.7~6	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin, 11:input from comparator
PD2MODE	0C.5~4	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin, 11:input from comparator
PD1MODE	0C.3~2	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin, 11:input from comparator
PD0MODE	0C.1~0	W	0	00:Pseudo open-drain, 01:Push-Pull output, 10:input from pin, 11:input from comparator
TESTreg	0F.3~0	W	0	Test Mode control, keep 0 in normal mode
TX0FIFO	18~1F	W	-	Endpoint 0 Transmit Buffer (8 Bytes)
TX1FIFO	20~27	W	-	Endpoint 1 Transmit Buffer (8 Bytes)
RC0ie	11.7	W	0	RC0 Interrupt enable
TX0ie	11.6	W	0	TX0 Interrupt enable
TX1ie	11.5	W	0	TX1 Interrupt enable
RSTie	11.3	W	0	USB Reset Interrupt enable
SUSPie	11.2	W	0	Suspend Interrupt enable
WKTie	11.1	W	0	WKT Interrupt enable
ALCe	12.5	W	0	Auto Level control enable(1:enable)
PS2kbd	12.4	W	0	Select PS2 Mode
RSMie	12.3	W	0	RSM Interrupt enable
PB0ie	12.1	W	0	PB[0] Interrupt enable
T0ie	12.0	W	0	Timer 0 Interrupt enable

9. Electrical Characteristics

ABSOLOUTE MAXIMUM RATINGS

GND= 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	-5 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	℃

RECOMMEND OPERATING CONDITION

at Ta=-20℃ to 70℃,GND= 0V

Name	Symb.	Min.	Max.	Unit
Supply Voltage	VDD	4.5	5.5	V

DC CHARACTERISTICS

at Ta=25 ℃,VDD=5.0V, VSS= 0V, Fosc=6MHz

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
Operating current	Icc		5.3		mA	Fosc=6MHz	
Suspend current	Isus	-	340	500	uA		No load
PB Output High Voltage	Vboh1	3.6	4.5	-	V	Ioh=5mA	Pseuso open-drain (Only one osc time)
		3.2	3.8	-	V	Ioh=12mA	
	Vboh2	3.2	4.0	-	V	Ioh=30uA	
		2.4	3.0	-	V	Ioh=50uA	
PB Output Low Voltage	Vbol	-	0.4	0.5	V	Iol=15mA	
		-	0.95	1.2	V	Iol=30mA	
PB Input High Voltage	Vbih	2.0	-	VDD	V		
PD Output High Voltage	Vdoh1	3.6	4.5	-	V	Ioh=5mA	PD push-pull / Pseudo open-drain (Only one osc time)
		3.2	3.8	-	V	Ioh=12mA	
	Vdoh2	3.2	4.0	-	V	Ioh=30uA	
PD Output Low voltage	Vdol1	-	0.4	0.5	V	Iol=8mA	PD[5:0] low sink
		-	0.95	1.2	V	Iol=16mA	
	Vdol2	-	0.4	0.5	V	Iol=16mA	PD[7:6] low sink
		-	0.95	1.2	V	Iol=30mA	
	Vdol3	-	0.4	0.5	V	Iol=30mA	PD[5:0] high sink
		-	0.95	1.2	V	Iol=60mA	
	Vdol4	-	0.4	0.5	V	Iol=50mA	PD[7:6] high sink
		-	0.95	1.2	V	Iol=100mA	
PD Input High Voltage	Vdih	2.5	-	VDD	V		

USB TIMING / ELECTRICAL CHARACTERISTICS

At Ta=25 ℃,VDD=5.0V, VSS= 0V, Fosc=6MHz

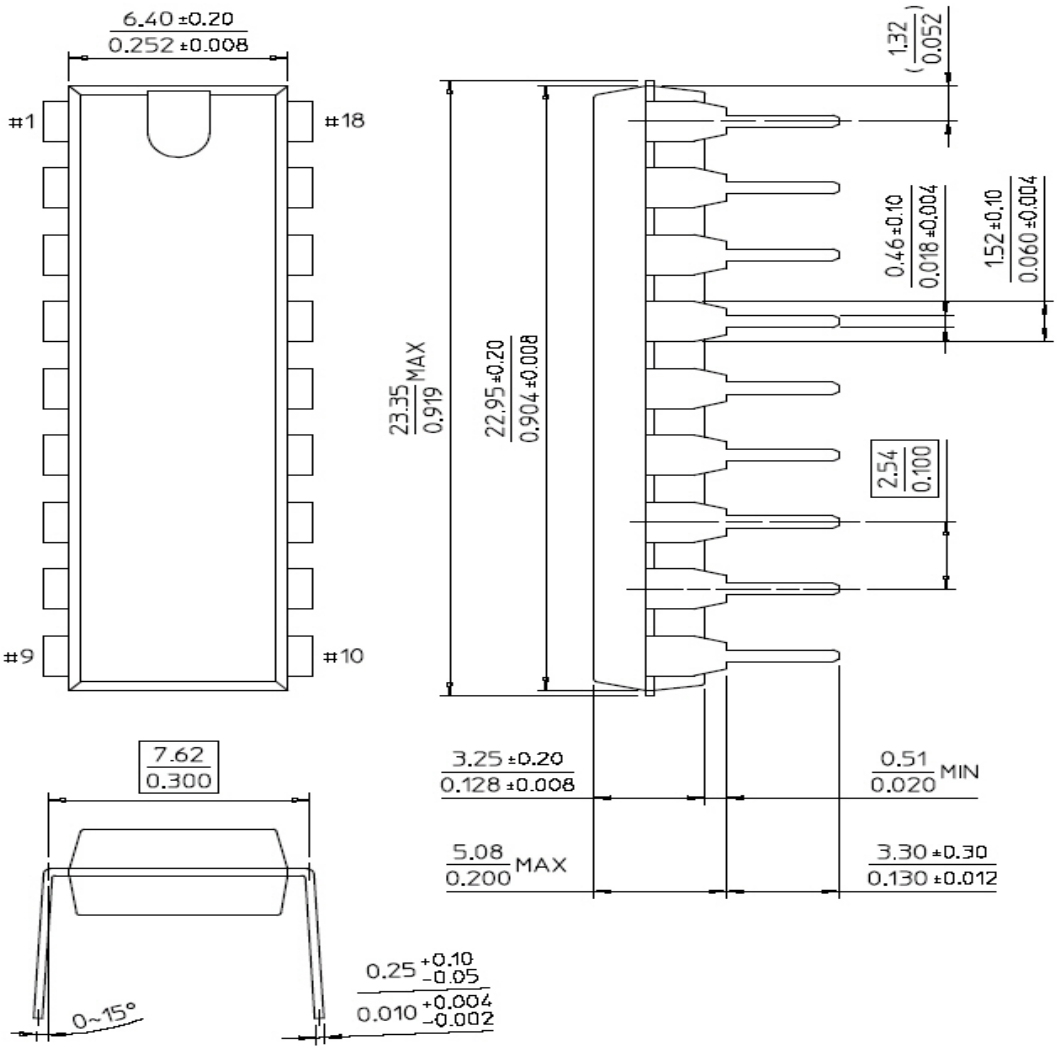
Name	Symb.	Min.	Max.	Unit	Note
DP/DM rising time	Trise	75	300	ns	C_L=390pF
DP/DM falling time	Tfall	75	300	ns	C_L=390pF
DP,DM cross point	Vx	1.3	2.0	V	
V33 output voltage	Vreg	3.2	3.4	V	
DM internal pull-high resistor		1.425	1.575	Kohm	

Note: All USB transceiver characteristics can meet USB1.1 spec.

10. Package Information

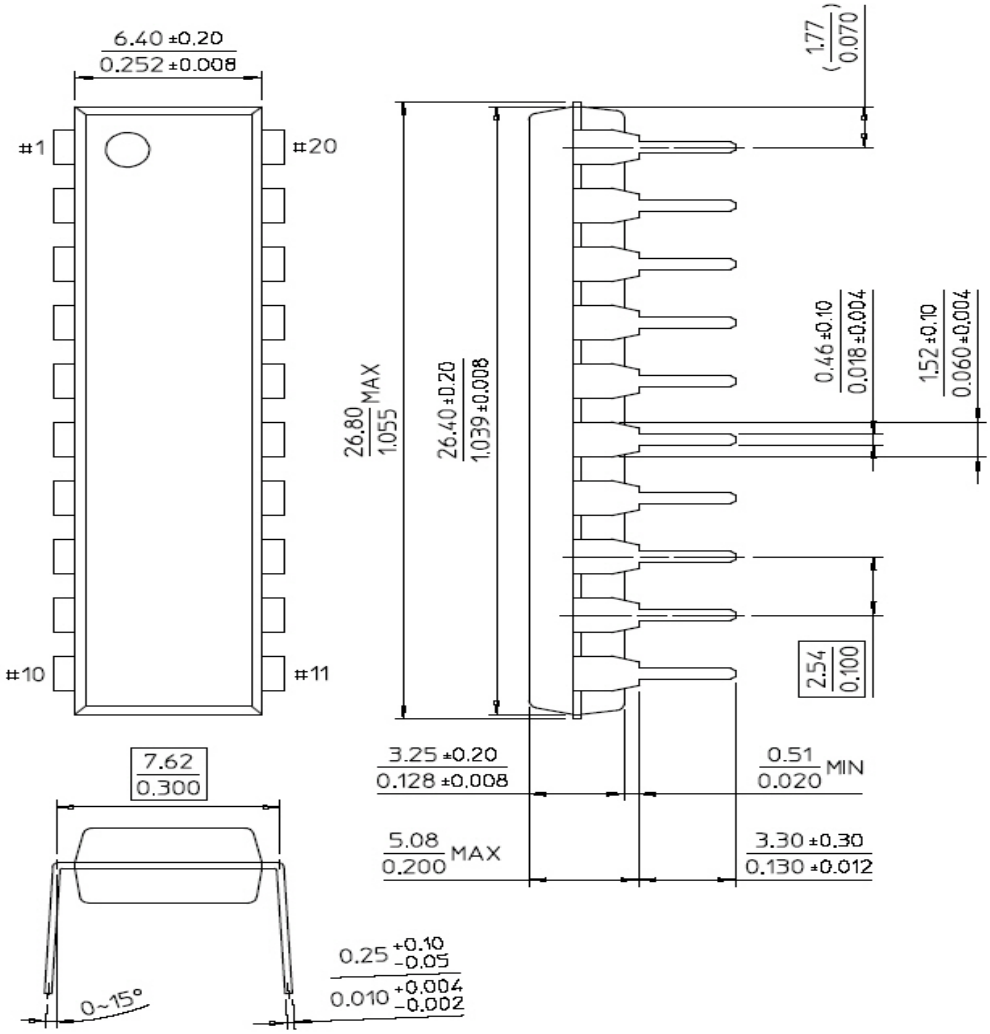
10.1 18 Pin DIP

Dimensions in Milimeters/inches



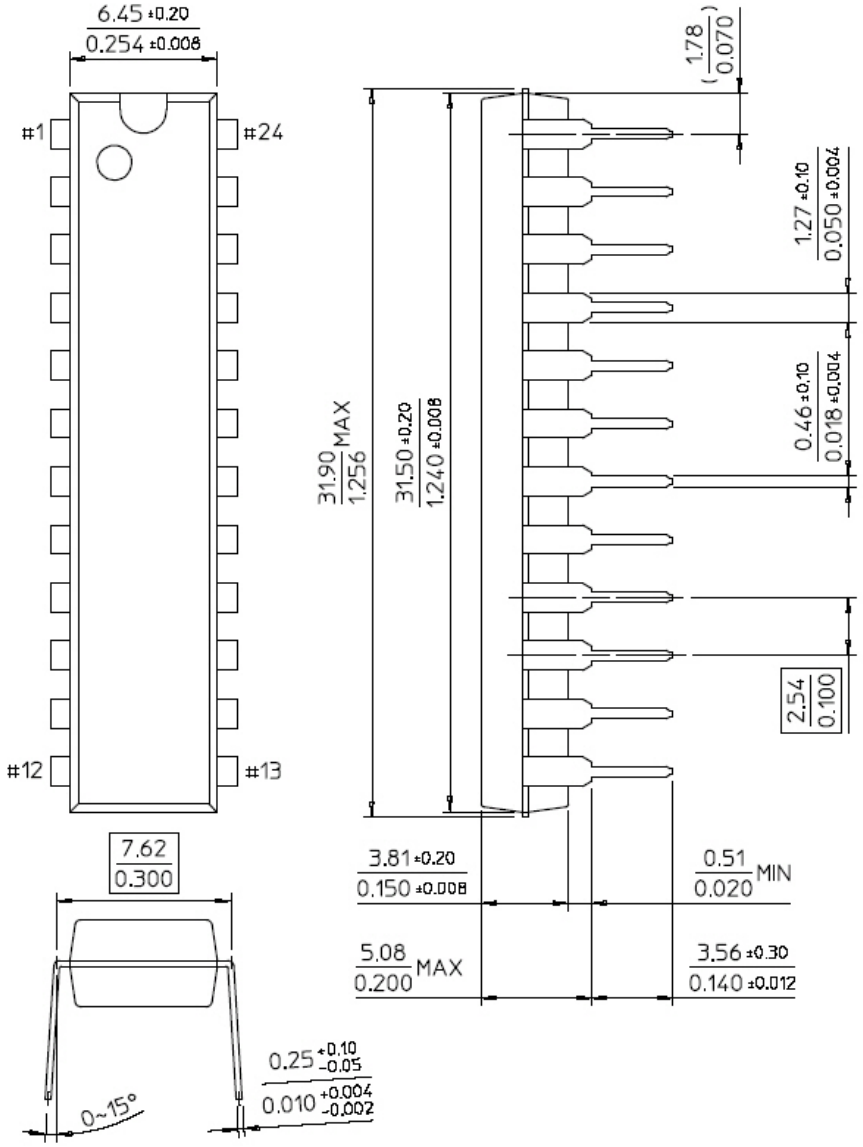
10.2 20 Pin Dip

Dimensions in Milimeters/inches

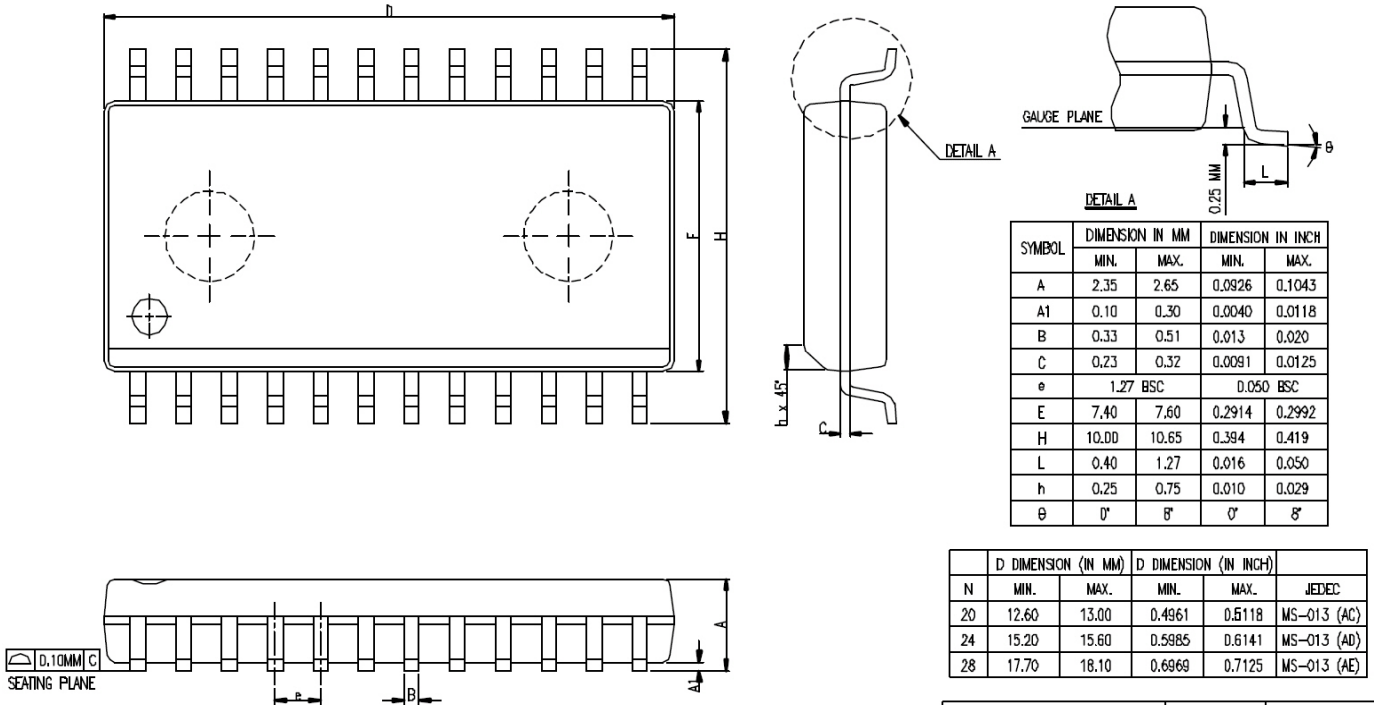


10.3 24 Pin DIP

Dimensions in Milimeters/inches



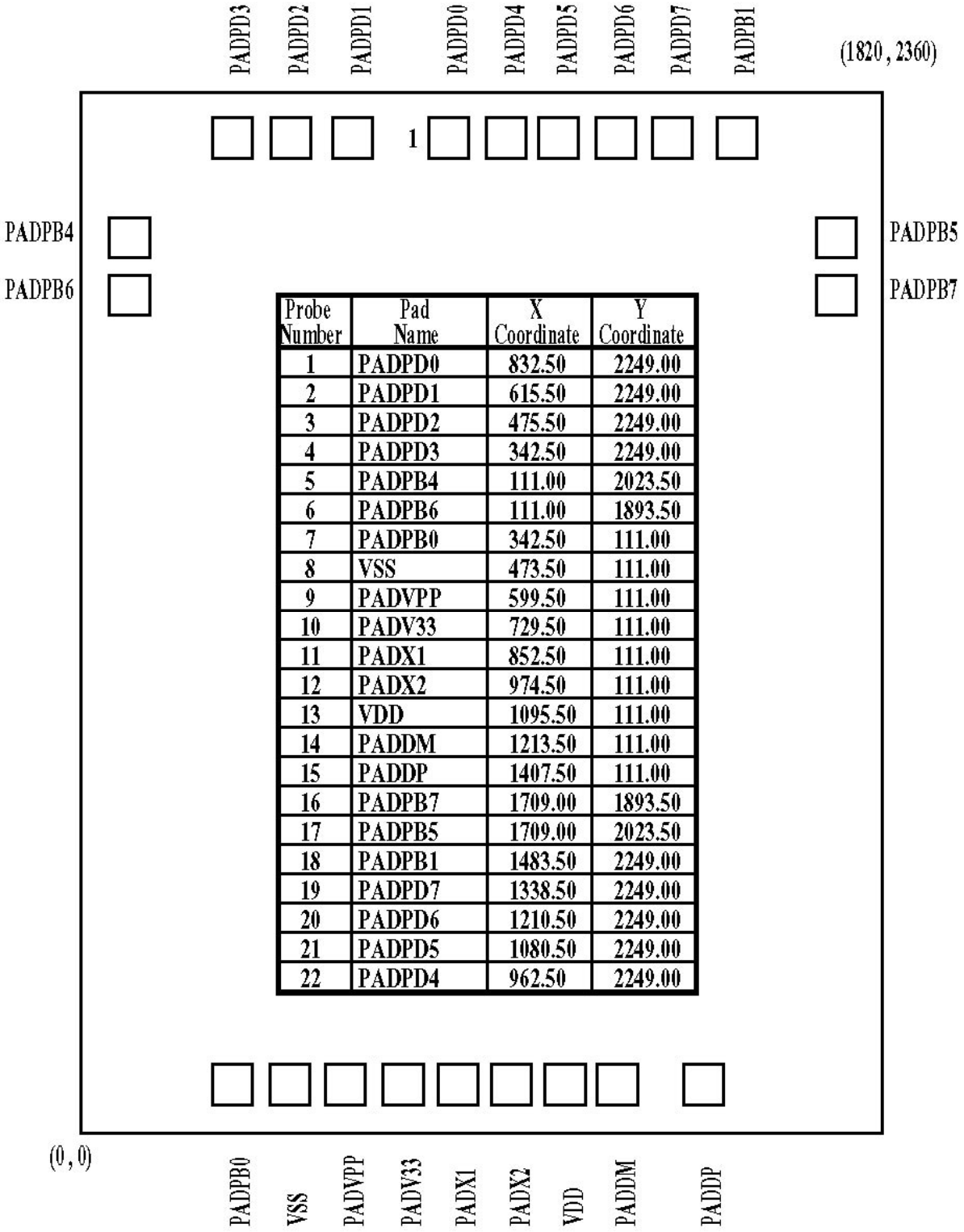
10.4 24 Pin SOP



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.0091	0.0125
e	1.27 BSC		0.050 BSC	
E	7.40	7.60	0.2914	0.2992
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

	D DIMENSION (IN MM)		D DIMENSION (IN INCH)		
N	MIN.	MAX.	MIN.	MAX.	JEDEC
20	12.60	13.00	0.4961	0.5118	MS-013 (AC)
24	15.20	15.60	0.5985	0.6141	MS-013 (AD)
28	17.70	18.10	0.6969	0.7125	MS-013 (AE)

10.5 Bonding Diagram



Probe Number	Pad Name	X Coordinate	Y Coordinate
1	PADPD0	832.50	2249.00
2	PADPD1	615.50	2249.00
3	PADPD2	475.50	2249.00
4	PADPD3	342.50	2249.00
5	PADPB4	111.00	2023.50
6	PADPB6	111.00	1893.50
7	PADPB0	342.50	111.00
8	VSS	473.50	111.00
9	PADVPP	599.50	111.00
10	PADV33	729.50	111.00
11	PADX1	852.50	111.00
12	PADX2	974.50	111.00
13	VDD	1095.50	111.00
14	PADDM	1213.50	111.00
15	PADDP	1407.50	111.00
16	PADPB7	1709.00	1893.50
17	PADPB5	1709.00	2023.50
18	PADPB1	1483.50	2249.00
19	PADPD7	1338.50	2249.00
20	PADPD6	1210.50	2249.00
21	PADPD5	1080.50	2249.00
22	PADPD4	962.50	2249.00

NOTE: The Programming PIN (VPP,VDD,PB0,PB1 ,DP,DM,X1,VSS)

11. Ordering Information

Ordering Code	Package Type	Operating Range
TMU3101CC	Chip	Commercial
TMU3101DC	18/20/24 Pin DIP Package	Commercial
TMU3101SC	18/20/24 Pin SOP Package	Commercial